R61505

262,144-color, 240RGB x 320 dot graphics liquid crystal controller driver for Amorphous-Silicon TFT Panel

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Description

The R61505 is a one-chip liquid crystal controller driver LSI for a-Si TFT panel, comprising RAM for a maximum 240 RGB x 320 dot graphics display, source driver, gate driver and power supply circuit. For the efficiency of data transfer, the R61505 supports high-speed interface via 8-/9-/16-/18-bit ports as system interface to microcomputer and high-speed RAM write function. As moving picture interface, the R61505 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0).

Also, the R61505 incorporates step-up circuit and voltage follower circuit to generate TFT liquid crystal panel drive voltages.

The R61505's power management functions such as 8-color display and deep standby and so on make this LSI an ideal driver for the medium or small sized portable products with color display system such as digital cellular phones or small PDAs, where long battery life is a major concern.

Features

- A one-chip controller driver incorporating a gate circuit and a power supply circuit for a maximum 240RGB x 320dots graphics display on amorphous TFT panel in 262k colors
- System interface
  - High-speed interfaces via 8-, 9-, 16-, 18-bit parallel ports
  - Clock synchronous serial interface
- Moving picture display interface
  - 6-, 16-, 18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  - VSYNC interface (System interface + VSYNC)
  - FMARK interface (System interface + FMARK)
- High-speed RAM write function
- Window address function to specify a rectangular area in the internal RAM to write data
- Write data within a rectangular area in the internal RAM via moving picture interface
- Reduce data transfer by specifying the area in the RAM to rewrite data
- Enable displaying the data in the still picture RAM area with a moving picture simultaneously
- Resizing function (x 1/2, x 1/4)
- Abundant color display and drawing functions
  - Programmable γ-correction function for 262k-color display
  - Partial display function
- Low -power consumption architecture (allowing direct input of interface I/O power supply)
  - Deep standby function
  - 8-color display function
  - Input power supply voltages: Vcc = 2.5V ~ 3.3 V (logic regulator power supply)
    IOVcc = 1.65V ~ 3.3 V (interface I/O power supply)
    Vci = 2.5V ~ 3.3 V (liquid crystal analog circuit power supply)
- Incorporates a liquid crystal drive power supply circuit
  - Source driver liquid crystal drive/Vcom power supply: DDVDH-GND = 4.5V ~ 6.0 V
    VCI-GND = -1.9V ~ -3.0V
    VCI-VCL ≤ 6V
  - Gate drive power supply: VGH-GND = 10.0V ~ 15.0 V
    VGL-GND = -4.5V ~ -12.5V
    VGH-VGL ≤ 25V
  - Vcom drive (Vcom power supply): VcomH = 3.0V ~ (DDVDH-0.5)V
    VcomL = (VCL+0.5)V ~ 0V
    VcomH-VcomL amplitude = 6.0V (max.)
- Liquid crystal power supply startup sequencer
- TFT storage capacitance: Cst only (common Vcom formula)
- 172,800-byte internal RAM
- Internal 720-channel source driver and 320-channel gate driver
- One-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate

Power Supply Specifications

Table 1

No.	Item		R61505
1	TFT data lines		720 output
2	TFT gate lines		320 output
3	TFT display storage capacitance		Cst only (Common Vcom formula)
4	Liquid crystal drive output	S1~S720	V0 ~ V31 grayscales
		G1~320	VGH-VGL
		Vcom	Change VcomH-VcomL amplitude with electronic volume Change VcomH with either electronic volume or from VcomR
5	Input voltage	IOVcc (interface voltage)	1.65V ~ 3.30V Power supply to IM0/ID, IM1-3, RESET*, DB17-0, RD*, SDI, SDO, WR/SCL, RS, CS*, VSYNC, HSYNC, DOTCLK, ENABLE, FMARK Connect to Vcc and Vci on the FPC when the electrical potentials are the same.
		Vcc (logic regulator power supply)see Note 1	2.50V ~ 3.30V Connect to IOVcc and Vci on the FPC when the electrical potentials are the same.
		Vci (liquid crystal drive power supply voltage)	2.50V ~ 3.30V Connect to IOVcc and Vcc on the FPC when the electrical potentials are the same.
6	Liquid crystal drive voltages	DDVDH	4.5V ~ 6.0V
		VGH	10.0V ~ 15.0V
		VGL	-4.5V ~ -12.5V
		VGH-VGL	Max. 25V
		VCL	-1.9V ~ -3.0V
		VCI-VCL	Max. 6.0V
6	Internal step-up circuits	VLOUT1 (DDVDH)	Vci1 x 2, x 3
		VLOUT2 (VGH)	Vci1 x 6, x 7, x 8
		VLOUT3 (VGL)	Vci1 x -3, x -4, x -5
		VCL	Vci1 x -1

Note: When using the internal logic regulator circuit.

Block Diagram

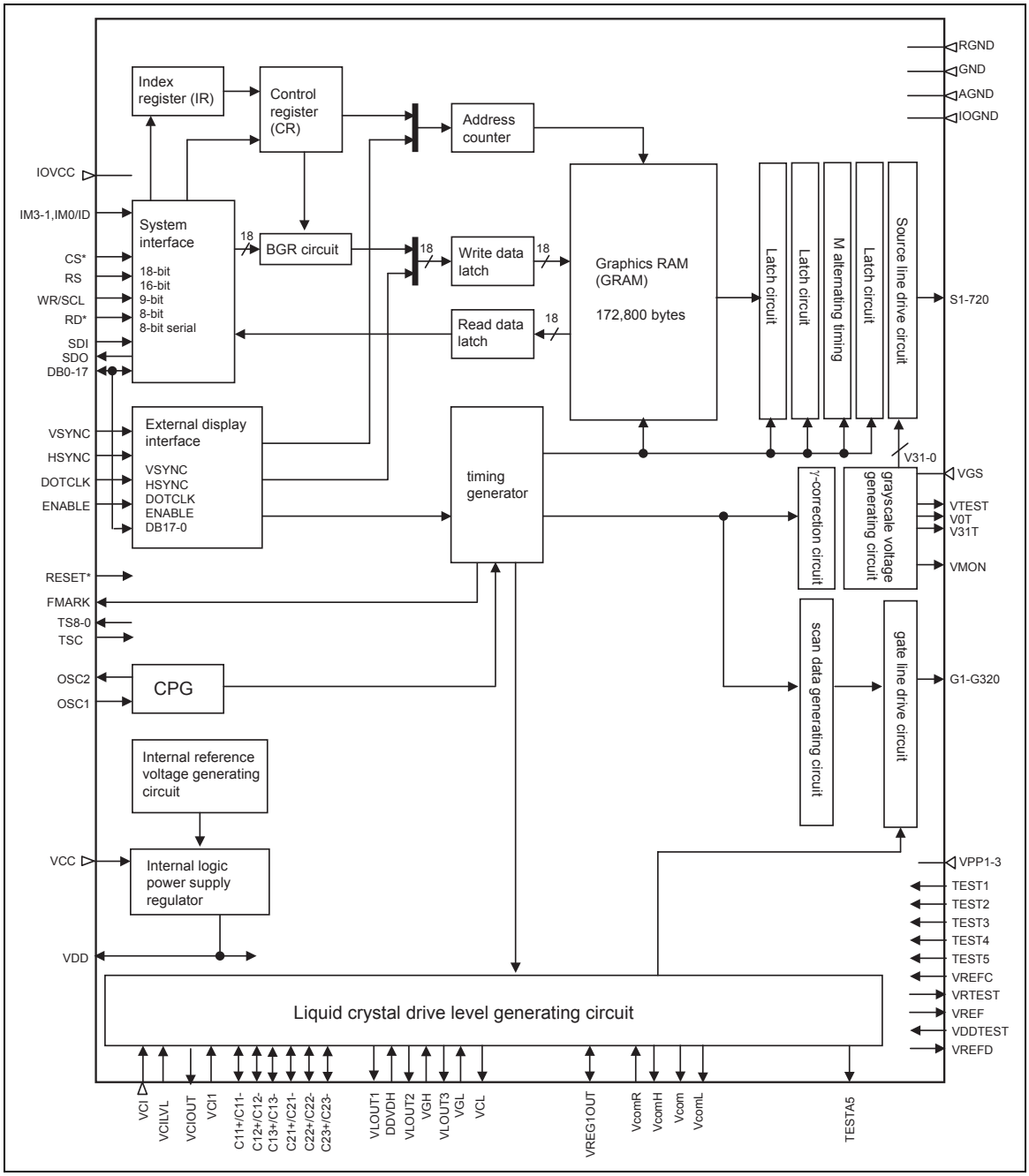


Figure 1

Block Function

1. System Interface

The R61505 supports 80-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and a clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The R61505 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control register and internal GRAM. The WDR is the register to temporarily store data to be written to control register and internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the R61505 performs the first read operation from the internal GRAM. Valid data is read out when the R61505 performs the second and subsequent read operation.

The instruction execution time except that of starting oscillation takes 0 clock cycle to allow writing instructions consecutively.

Table 2 Register Selection (80-system 8/9/16/18-bit Parallel Interface)

WR*	RD*	RS	Function
0	1	0	Write index to IR
1	0	0	Setting disabled
0	1	1	Write to control registers or internal GRAM via WDR
1	0	1	Read from internal GRAM via RDR

Table 3 Register Selection (Serial Interface)

Start Byte		
R/W	RS	Function
0	0	Write index to IR
1	0	Setting disabled
0	1	Write to control registers or internal GRAM via WDR
1	1	Read from internal GRAM via RDR

Table 4

IM3	IM2	IM1	IM0	System Interface	DB Pins	RAM Write Data	Instruction Write Transfer
0	0	0	0	Setting disabled	-	-	-
0	0	0	1	Setting disabled	-	-	-
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	Single transfer (16 bits) 2 transfers (1st: 2 bits, 2nd: 16 bits) 2 transfers (1st: 16 bits, 2nd: 2 bits)	Single transfer (16 bits)
0	0	1	1	80-system 8-bit interface	DB17-10	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	0	*	Clock synchronous serial interface	- (SDI, SDO)	2 transfers (1st: 8 bits, 2nd: 8 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	1	0	Setting disabled	-	-	-
0	1	1	1	Setting disabled	-	-	-
1	0	0	0	Setting disabled	-	-	-
1	0	0	1	Setting disabled	-	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	Single transfer (18 bits)	Single transfer (16 bits)
1	0	1	1	80-system 9-bit interface	DB17-9	2 transfers (1st: 9 bits, 2nd: 9 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
1	1	*	*	Setting disabled		-	-

2. External Display Interface (RGB, VSYNC Interfaces)

The R61505 supports RGB interface and VSYNC interface as the external interface to display moving picture. When the RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB17-0) is written in synchronization with these signals when the polarity of enable signal (ENABLE) allows write operation in order to prevent flicker while updating display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, which synchronizes the display operation with the VSYNC signal. The display data is written to the internal GRAM via system interface. When writing data via VSYNC interface, there are constraints in speed and method in writing data to the internal RAM. For details, see the “VSYNC interface” section.

The R61505 allows switching interface by instruction according to the display, i.e. still and/or moving picture(s). The R61505 writes all display data via RGB interface to the internal GRAM in order to transfer data only when updating the data and thereby reduce the data transfer and power consumption for moving picture display.

3. Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register to set a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As the R61505 writes data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only within the rectangular area specified in the GRAM.

4. Graphics RAM (GRAM)

GRAM is graphics RAM, which can store bit-pattern data of 172,800 (240RGB x 320 (dots) x 18(bits)) bytes at maximum, using 18 bits per pixel.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltages according to the grayscale data in the γ-correction registers to enable 262k-color display. For details, see the γ-Correction Register section.

6. Liquid Crystal Drive Power Supply Circuit

The liquid crystal drive power supply circuit generates VDH, VGH, VGL and Vcom levels to drive liquid crystal.

7. Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal GRAM. The timing signal for display operation such as RAM read operation and the timing signal for internal operation such as RAM access from the MPU are generated separately in order to avoid mutual interference.

8. Oscillator (OSC)

The R61505 generates the RC oscillation clock just by connecting an external oscillation resistor between the OSC1 and OSC2 pins. The oscillation frequency can be changed by changing the resistance of the external resistor. Adjust the oscillation frequency according to operating voltage and frame frequency. While the R61505 is in deep standby mode, RC oscillation is halted to reduce power consumption. For details, see “Oscillator”.

9. Liquid Crystal Driver Circuit

The liquid crystal driver circuit of the R61505 consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). The display pattern data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the SS bit and the shift direction of gate output from the gate driver can be changed by setting the GS bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

10. Internal Logic Power Supply Regulator

The internal logic power supply regulator generates internal logic power supply VDD.

Pin Function

Table 5

<table>
<tr><th>Signal</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in Use</th></tr>
<tr><td>IM3-1, IM0/ID</td><td>I</td><td>IOGND or IOVcc</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 see Note 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 see Note 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>65,536</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table>
Notes: 1. 65,536 colors in one transfer mode
2. 65,536 colors in two transfers mode</td><td>-</td></tr>
<tr><td>CS*</td><td>I</td><td>MPU</td><td>Chip select signal. Amplitude: IOVcc-IOGND
Low: the R61505 is selected and accessible
High: the R61505 is not selected and not accessible.</td><td>IOVCC</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal. Amplitude: IOVcc-IOGND
Low: select Index or status register
High: select control register</td><td>IOVcc</td></tr>
<tr><td>WR*/SCL</td><td>I</td><td>MPU</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when WR* is low. Synchronous clock signal (SCL) in serial interface operation. Amplitude: IOVcc-IOGND</td><td>IOVcc</td></tr>
<tr><td>RD*</td><td>I</td><td>MPU</td><td>Read strobe signal in 80-system bus interface operation and enables read operation when RD* is low. Amplitude: IOVcc-IOGND</td><td>IOVcc</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>Serial data input (SDI) pin in serial interface operation. The data is inputted on the rising edge of the SCL signal. Amplitude: IOVcc-IOGND</td><td>IOGND or IOVcc</td></tr>
<tr><td>SDO</td><td>I/O</td><td>MPU</td><td>Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal.
Amplitude: IOVcc-IOGND</td><td>Open</td></tr>
</table>

Signal	I/O	Connect to	Function	When not in Use
DB0-DB17	I/O	MPU	18-bit parallel bi-directional data bus for 80-system interface operation (Amplitude: IOVcc-IOGND). 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-1 are used. 18-bit I/F: DB17-DB0 are used. 18-bit parallel bi-directional data bus for RGB interface operation (Amplitude: IOVcc-IOGND). 6-bit I/F: DB17-DB12 are used. 16-bit I/F: DB17-DB13 and DB11-1 are used. 18-bit I/F: DB17-DB0 are used.	IOGND or IOVcc
ENABLE	I	MPU	Data enable signal for RGB interface operation. (Amplitude: IOVcc-IOGND). Low: accessible (select) High: Note accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit.	IOGND or IOVcc
VSYNC	I	MPU	Frame synchronous signal for RGB interface operation. Low active. (Amplitude: IOVcc-IOGND).	IOGND or IOVcc
HSYNC	I	MPU	Line synchronous signal for RGB interface operation. Low active. (Amplitude: IOVcc-IOGND).	IOGND or IOVcc
DOTCLK	I	MPU	Dot clock signal for RGB interface operation. The data input timing is on the rising edge of DOTCLK. (Amplitude: IOVcc-IOGND).	IOGND or IOVcc
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM. (Amplitude: IOVcc-IOGND).	Open
RESET*	I	MPU or external RC circuit	Reset signal. Initializes the R61505 when it is low. Make sure to execute a power-on reset when turning on power supply (IOVCC-IOGND amplitude signal).	-
OSC1 OSC2	I O	Oscillator	Connect an external resistor for RC oscillation.	-
Vcc	-	Power supply	Power supply to internal logic regulator circuit: Vcc = 2.5V~3.3V. Vcc ≥ IOVcc	-
GND	-	Power supply	Internal logic GND: GND = 0V.	-
RGND	-	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.	-
VDD	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.	-
IOVcc	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVcc = 1.65V ~ 3.3V. Vcc ≥ IOVcc. In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.	-
IOGND	-	Power supply	GND for the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.	-

Signal	I/O	Connect to	Function	When not in Use
AGND	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.	-
Vci	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.	-
VciLVL	I	Reference power supply	VciLVL must be at the same electrical potential as Vci. VciLVL = 2.5V ~ 3.3V. Connect to external power supply. In case of COG, connect to Vci on the FPC to prevent noise.	-
VciOUT	O	Stabilizing capacitor, Vci1	Internal reference voltage generated between Vci and GND. The output level is set by instruction (VC bits).	-
Vci1	I/O	VciOUT	Reference voltage for the step-up circuit 1. Make sure to set the Vci1 voltage so that VLOUT1, VLOUT2 and VLOUT3 voltages are set within the respective ranges.	-
VLOUT1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1, generated from Vci1. The step-up factor is set by instruction (BT bits). VLOUT1 = 4.5V ~ 6.0V	-
DDVDH	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and Vcom drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V	-
VLOUT2	O	Stabilizing capacitor, VGH	Output voltage from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor is set by instruction (BT bits). VLOUT2 = max 15.0V	-
VGH	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.	-
VLOUT3	O	Stabilizing capacitor, VGL	Output voltage from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor is set by instruction (BT bits). VLOUT3 = min –12.5V	-
VGL	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.	-
VCL	O	Stabilizing capacitor	VCOML drive power supply. VCL = -1.9V ~ -3.0V	-
C11+, C11- C12+, C12-	I O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.	-
C13+, C13- C21+, C21- C22+, C22- C23+, C23-	I O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.	-
VREG1 OUT	O	Stabilizing capacitor	Output voltage generated from the reference voltage. The factor is determined by instruction (VRH bits). VREG1OUT is used for (1) source driver grayscale reference voltage VDH, (2) VcomH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor when in use. VREG1OUT = 3.0V ~ (DDVDH – 0.5)V When the load is on current to the maximum, VREG1OUT = 3.0V ~ (DDVDH – 0.3) is also possible.	Open
Vcom	O	TFT panel common electrode	Power supply to TFT panel's common electrode. Vcom alternates between VcomH and VcomL. The alternating cycle is set by internal register. Also, the Vcom output can be started and halted by register setting.	Open

Signal	I/O	Connect to	Function	When not in Use
VcomH	O	Stabilizing capacitor	The High level of Vcom amplitude. The output level can be adjusted by either external resistor (VcomR) or electronic volume.	Open
VcomL	O	Stabilizing capacitor	The Low level of Vcom amplitude. The output level can be adjusted by instruction (VDV bits). VcomL = (VCL+0.5)V ~ 0V	Open
VcomR	I	Variable resistor or open	Connect a variable resistor when adjusting the VcomH level between VREG1OUT and GND.	Open
VGS	I	GND	Reference level for the grayscale voltage generating circuit.	-
S1~S720	O	LCD	Liquid crystal application voltages. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is outputted from S1. When SS = 1, the data in the RAM address h00000 is outputted from S720.	Open
G1~G320	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level	Open
V0T, V31T	I/O	Open	Test pins. Leave them open.	Open
VTEST	O	Open	Test pin. Leave it open.	Open
VREFC	I	AGND	Test pin. Make sure to fix to the AGND level.	-
VREF	O	Open	Test pin. Leave it open.	Open
VDDTEST	I	AGND	Test pin. Make sure to fix to the AGND level.	-
VREFD	O	Open	Test pin. Leave it open.	Open
VMON	O	Open	Test pin. Leave it open.	Open
TESTA5	O	Open	Test pin. Leave it open.	Open
IOVCCDUM1-2	O	-	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.	Open
VCCDUM1	O	-	Test pin. Leave it open	Open
IOGNDDUM1-3	O	-	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.	Open
OSC1DUM1-4	O	-	Test pins. Leave them open.	Open
OSC2DUM1-2	O	-	Test pins. Leave them open.	Open
AGNDDUM1-4	O	-	Use them to fix VREFC, VDDTEST.	Open
DUMMYR 1-10	-	-	DUMMYR1 and DUMMYR10, DUMMYR2 and DUMMYR9, DUMMYR3 and DUMMYR4, DUMMYR5 and DUMMYR8, and DUMMYR6 and DUMMYR7 are short-circuited within the chip for COG contact resistance measurement.	Open
VGLDMY 1-4	O	-	Dummy pads. Leave them open.	Open

Signal	I/O	Connect to	Function	When not in Use
TESTO1-38	O	-	Dummy pads. Leave them open.	Open
TEST1, 2, 5	I	IOGND	Test pins. Connect to IOGND.	IOGND
TEST3	I	IOVcc	Test pin. Connect to IOVcc.	IOVcc
TEST4	I	IOVcc	Test pin. Connect to IOVcc on the FPC.	IOVcc
TSC	I	AGND	Test pin. Connect to IOGND.	IOGND
TS8-0	O	Open	Test pins. Leave them open.	Open
VPP1-3	-	Power supply	Test pins. Leave them open.	Open

Patents of dummy pin which is used to fix pin to VCC or GND are pending or granted.

PATENT ISSUED: United States Patent No. 6,323,930
PATENT PENDING: Japanese Application No. 10-514484, Korean Application No. 19997002322
Taiwanese Application No.086103756, (PCT/JP96/02728(W098/12597)

R61505 PAD arrangement

Rev1.2 2005.07.01

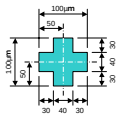
●Chip size: 21.58mm× 1.87mm
●Chip thickness: 400μm(typ.)
●PAD coordinates: PAD center
●Coordinates origin: Chip center

●Au BUMP size:
(1) 50.00 μm x 80.00μm
No.1 - 298

(2) 21.00μm x 100.00μm
No.299 - 1354

●Au BUMP pitch: See PAD coordinates Table
●Au BUMP height: 15μm(typ.)
●No. in the Figure corresponds to No. in PAD coordinates Table

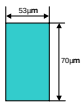
●Alignment mark
(1-a), (1-b)



(2-a)

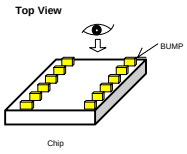
(2-b)

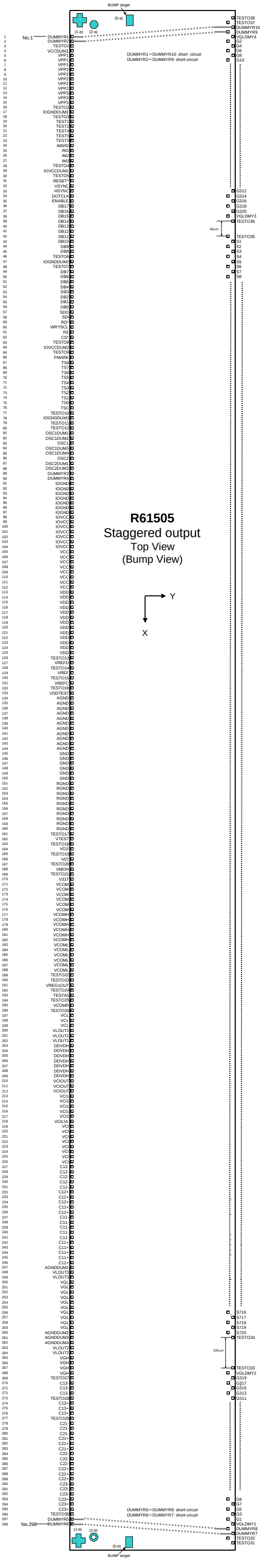
●BUMP target cell:



(3) Coordinates: 2 positions
(5-a)
(5-b)

Top View



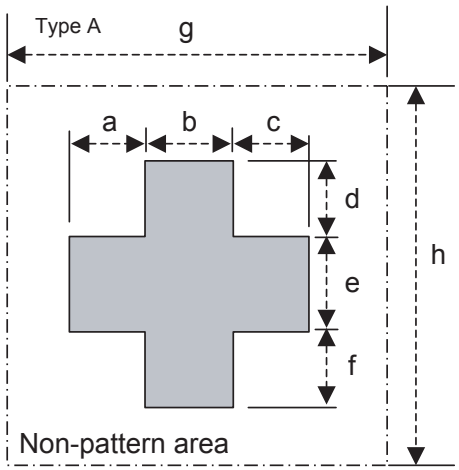


- Chip size: 21.58 mm x 1.87 mm
- Chip thickness: 400μm (typ.)
- PAD coordinates: PAD center
- PAD coordinates origin: Chip center
- Au bump size

(1) 50μm× 80μm
I/O output side:
No. 1 - No. 298

(2) 21μm× 100μm
Liquid crystal output side:
No. 299 - No. 1354

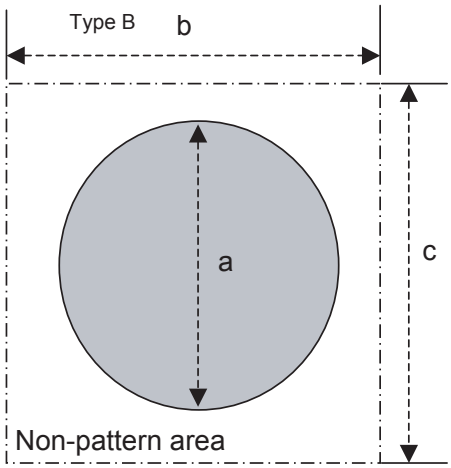
- Au bump pitch: See PAD coordinates table
- Au bump height: 15μm(typ.)
- No. in the Figure corresponds to No. in the PAD coordinates table



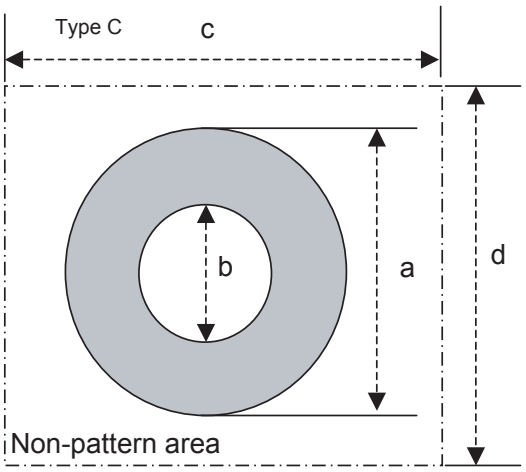
Unit (μm)
a: 30 e: 40
b: 40 f: 30
c: 30 g: 100
d: 30 h: 100

- Alignment mark

Alignment mark shape	X	Y
Type A	-10613.0	-753.0
	10613.0	-753.0
Type B	-10572.0	-613.0
Type C	10572.0	-613.0



Unit (μm)
a: 50
b: 90
c: 90



Unit (μm)
a: 50
b: 20
c: 90
d: 90

R61505 PAD coordinates (Unit: μm) 2005.08.24 rev1.2

pad No	pad name	X	Y
1	DUMMYR1	-10395.0	-801.5
2	DUMMYR2	-10325.0	-801.5
3	TESTO1	-10255.0	-801.5
4	VCCDUM1	-10185.0	-801.5
5	VPP1	-10115.0	-801.5
6	VPP1	-10045.0	-801.5
7	VPP1	-9975.0	-801.5
8	VPP2	-9905.0	-801.5
9	VPP2	-9835.0	-801.5
10	VPP2	-9765.0	-801.5
11	VPP2	-9695.0	-801.5
12	VPP2	-9625.0	-801.5
13	VPP3	-9555.0	-801.5
14	VPP3	-9485.0	-801.5
15	VPP3	-9415.0	-801.5
16	TESTO2	-9345.0	-801.5
17	IOGNDDUM1	-9275.0	-801.5
18	TESTO3	-9205.0	-801.5
19	TEST1	-9135.0	-801.5
20	TEST2	-9065.0	-801.5
21	TEST4	-8995.0	-801.5
22	TEST5	-8925.0	-801.5
23	TEST3	-8855.0	-801.5
24	IM0/ID	-8785.0	-801.5
25	IM1	-8715.0	-801.5
26	IM2	-8645.0	-801.5
27	IM3	-8575.0	-801.5
28	TESTO4	-8505.0	-801.5
29	IOVCCDUM1	-8435.0	-801.5
30	TESTO5	-8365.0	-801.5
31	RESET*	-8295.0	-801.5
32	VSYNC	-8225.0	-801.5
33	HSYNC	-8155.0	-801.5
34	DOTCLK	-8085.0	-801.5
35	ENABLE	-8015.0	-801.5
36	DB17	-7945.0	-801.5
37	DB16	-7875.0	-801.5
38	DB15	-7805.0	-801.5
39	DB14	-7735.0	-801.5
40	DB13	-7665.0	-801.5
41	DB12	-7595.0	-801.5
42	DB11	-7525.0	-801.5
43	DB10	-7455.0	-801.5
44	DB9	-7385.0	-801.5
45	DB8	-7315.0	-801.5
46	TESTO6	-7245.0	-801.5
47	IOGNDDUM2	-7175.0	-801.5
48	TESTO7	-7105.0	-801.5
49	DB7	-7035.0	-801.5
50	DB6	-6965.0	-801.5

pad No	pad name	X	Y
51	DB5	-6895.0	-801.5
52	DB4	-6825.0	-801.5
53	DB3	-6755.0	-801.5
54	DB2	-6685.0	-801.5
55	DB1	-6615.0	-801.5
56	DB0	-6545.0	-801.5
57	SDO	-6475.0	-801.5
58	SDI	-6405.0	-801.5
59	RD*	-6335.0	-801.5
60	WR*/SCL	-6265.0	-801.5
61	RS	-6195.0	-801.5
62	CS*	-6125.0	-801.5
63	TESTO8	-6055.0	-801.5
64	IOVCCDUM2	-5985.0	-801.5
65	TESTO9	-5915.0	-801.5
66	FMARK	-5845.0	-801.5
67	TS8	-5775.0	-801.5
68	TS7	-5705.0	-801.5
69	TS6	-5635.0	-801.5
70	TS5	-5565.0	-801.5
71	TS4	-5495.0	-801.5
72	TS3	-5425.0	-801.5
73	TS2	-5355.0	-801.5
74	TS1	-5285.0	-801.5
75	TS0	-5215.0	-801.5
76	TSC	-5145.0	-801.5
77	TESTO10	-5075.0	-801.5
78	IOGNDDUM3	-5005.0	-801.5
79	TESTO11	-4935.0	-801.5
80	TESTO12	-4865.0	-801.5
81	OSC1DUM1	-4795.0	-801.5
82	OSC1DUM2	-4725.0	-801.5
83	OSC1	-4655.0	-801.5
84	OSC1DUM3	-4585.0	-801.5
85	OSC1DUM4	-4515.0	-801.5
86	OSC2	-4445.0	-801.5
87	OSC2DUM1	-4375.0	-801.5
88	OSC2DUM2	-4305.0	-801.5
89	DUMMYR3	-4235.0	-801.5
90	DUMMYR4	-4165.0	-801.5
91	IOGND	-4095.0	-801.5
92	IOGND	-4025.0	-801.5
93	IOGND	-3955.0	-801.5
94	IOGND	-3885.0	-801.5
95	IOGND	-3815.0	-801.5
96	IOGND	-3745.0	-801.5
97	IOGND	-3675.0	-801.5
98	IOVCC	-3605.0	-801.5
99	IOVCC	-3535.0	-801.5
100	IOVCC	-3465.0	-801.5

R61505 PAD coordinates (Unit: μm) 2005.08.24 rev1.2

pad No	pad name	X	Y
101	IOVCC	-3395.0	-801.5
102	IOVCC	-3325.0	-801.5
103	IOVCC	-3255.0	-801.5
104	IOVCC	-3185.0	-801.5
105	VCC	-3115.0	-801.5
106	VCC	-3045.0	-801.5
107	VCC	-2975.0	-801.5
108	VCC	-2905.0	-801.5
109	VCC	-2835.0	-801.5
110	VCC	-2765.0	-801.5
111	VCC	-2695.0	-801.5
112	VCC	-2625.0	-801.5
113	VDD	-2555.0	-801.5
114	VDD	-2485.0	-801.5
115	VDD	-2415.0	-801.5
116	VDD	-2345.0	-801.5
117	VDD	-2275.0	-801.5
118	VDD	-2205.0	-801.5
119	VDD	-2135.0	-801.5
120	VDD	-2065.0	-801.5
121	VDD	-1995.0	-801.5
122	VDD	-1925.0	-801.5
123	VDD	-1855.0	-801.5
124	VDD	-1785.0	-801.5
125	VDD	-1715.0	-801.5
126	TESTO13	-1645.0	-801.5
127	VREFD	-1575.0	-801.5
128	TESTO14	-1505.0	-801.5
129	VREF	-1435.0	-801.5
130	TESTO15	-1365.0	-801.5
131	VREFC	-1295.0	-801.5
132	TESTO16	-1225.0	-801.5
133	VDDTEST	-1155.0	-801.5
134	AGND	-1085.0	-801.5
135	AGND	-1015.0	-801.5
136	AGND	-945.0	-801.5
137	AGND	-875.0	-801.5
138	AGND	-805.0	-801.5
139	AGND	-735.0	-801.5
140	AGND	-665.0	-801.5
141	AGND	-595.0	-801.5
142	AGND	-525.0	-801.5
143	AGND	-455.0	-801.5
144	AGND	-385.0	-801.5
145	GND	-315.0	-801.5
146	GND	-245.0	-801.5
147	GND	-175.0	-801.5
148	GND	-105.0	-801.5
149	GND	-35.0	-801.5
150	GND	35.0	-801.5

pad No	pad name	X	Y
151	RGND	105.0	-801.5
152	RGND	175.0	-801.5
153	RGND	245.0	-801.5
154	RGND	315.0	-801.5
155	RGND	385.0	-801.5
156	RGND	455.0	-801.5
157	RGND	525.0	-801.5
158	RGND	595.0	-801.5
159	RGND	665.0	-801.5
160	RGND	735.0	-801.5
161	TESTO17	805.0	-801.5
162	VTEST	875.0	-801.5
163	TESTO18	945.0	-801.5
164	VGS	1015.0	-801.5
165	TESTO19	1085.0	-801.5
166	V0T	1155.0	-801.5
167	TESTO20	1225.0	-801.5
168	VMON	1295.0	-801.5
169	TESTO21	1365.0	-801.5
170	V31T	1435.0	-801.5
171	VCOM	1505.0	-801.5
172	VCOM	1575.0	-801.5
173	VCOM	1645.0	-801.5
174	VCOM	1715.0	-801.5
175	VCOM	1785.0	-801.5
176	VCOM	1855.0	-801.5
177	VCOMH	1925.0	-801.5
178	VCOMH	1995.0	-801.5
179	VCOMH	2065.0	-801.5
180	VCOMH	2135.0	-801.5
181	VCOMH	2205.0	-801.5
182	VCOMH	2275.0	-801.5
183	VCOML	2345.0	-801.5
184	VCOML	2415.0	-801.5
185	VCOML	2485.0	-801.5
186	VCOML	2555.0	-801.5
187	VCOML	2625.0	-801.5
188	VCOML	2695.0	-801.5
189	TESTO22	2765.0	-801.5
190	TESTO23	2835.0	-801.5
191	VREG1OUT	2905.0	-801.5
192	TESTO24	2975.0	-801.5
193	TESTA5	3045.0	-801.5
194	TESTO25	3115.0	-801.5
195	VCOMR	3185.0	-801.5
196	TESTO26	3255.0	-801.5
197	VCL	3325.0	-801.5
198	VCL	3395.0	-801.5
199	VCL	3465.0	-801.5
200	VLOUT1	3535.0	-801.5

R61505 PAD coordinates (Unit: μm) 2005.08.24 rev1.2

pad No	pad name	X	Y
201	VLOUT1	3605.0	-801.5
202	VLOUT1	3675.0	-801.5
203	DDVDH	3745.0	-801.5
204	DDVDH	3815.0	-801.5
205	DDVDH	3885.0	-801.5
206	DDVDH	3955.0	-801.5
207	DDVDH	4025.0	-801.5
208	DDVDH	4095.0	-801.5
209	DDVDH	4165.0	-801.5
210	VCIOUT	4235.0	-801.5
211	VCIOUT	4305.0	-801.5
212	VCIOUT	4375.0	-801.5
213	VCI1	4445.0	-801.5
214	VCI1	4515.0	-801.5
215	VCI1	4585.0	-801.5
216	VCI1	4655.0	-801.5
217	VCI1	4725.0	-801.5
218	VCILVL	4795.0	-801.5
219	VCI	4865.0	-801.5
220	VCI	4935.0	-801.5
221	VCI	5005.0	-801.5
222	VCI	5075.0	-801.5
223	VCI	5145.0	-801.5
224	VCI	5215.0	-801.5
225	VCI	5285.0	-801.5
226	VCI	5355.0	-801.5
227	C12-	5425.0	-801.5
228	C12-	5495.0	-801.5
229	C12-	5565.0	-801.5
230	C12-	5635.0	-801.5
231	C12-	5705.0	-801.5
232	C12+	5775.0	-801.5
233	C12+	5845.0	-801.5
234	C12+	5915.0	-801.5
235	C12+	5985.0	-801.5
236	C12+	6055.0	-801.5
237	C11-	6125.0	-801.5
238	C11-	6195.0	-801.5
239	C11-	6265.0	-801.5
240	C11-	6335.0	-801.5
241	C11-	6405.0	-801.5
242	C11+	6475.0	-801.5
243	C11+	6545.0	-801.5
244	C11+	6615.0	-801.5
245	C11+	6685.0	-801.5
246	C11+	6755.0	-801.5
247	AGNDDUM1	6825.0	-801.5
248	VLOUT3	6895.0	-801.5
249	VLOUT3	6965.0	-801.5
250	VGL	7035.0	-801.5

pad No	pad name	X	Y
251	VGL	7105.0	-801.5
252	VGL	7175.0	-801.5
253	VGL	7245.0	-801.5
254	VGL	7315.0	-801.5
255	VGL	7385.0	-801.5
256	VGL	7455.0	-801.5
257	VGL	7525.0	-801.5
258	VGL	7595.0	-801.5
259	VGL	7665.0	-801.5
260	AGNDDUM2	7735.0	-801.5
261	AGNDDUM3	7805.0	-801.5
262	AGNDDUM4	7875.0	-801.5
263	VLOUT2	7945.0	-801.5
264	VLOUT2	8015.0	-801.5
265	VGH	8085.0	-801.5
266	VGH	8155.0	-801.5
267	VGH	8225.0	-801.5
268	VGH	8295.0	-801.5
269	TESTO27	8365.0	-801.5
270	C13-	8435.0	-801.5
271	C13-	8505.0	-801.5
272	C13-	8575.0	-801.5
273	TESTO28	8645.0	-801.5
274	C13+	8715.0	-801.5
275	C13+	8785.0	-801.5
276	C13+	8855.0	-801.5
277	TESTO29	8925.0	-801.5
278	C21-	8995.0	-801.5
279	C21-	9065.0	-801.5
280	C21-	9135.0	-801.5
281	C21+	9205.0	-801.5
282	C21+	9275.0	-801.5
283	C21+	9345.0	-801.5
284	C22-	9415.0	-801.5
285	C22-	9485.0	-801.5
286	C22-	9555.0	-801.5
287	C22+	9625.0	-801.5
288	C22+	9695.0	-801.5
289	C22+	9765.0	-801.5
290	C23-	9835.0	-801.5
291	C23-	9905.0	-801.5
292	C23-	9975.0	-801.5
293	C23+	10045.0	-801.5
294	C23+	10115.0	-801.5
295	C23+	10185.0	-801.5
296	TESTO30	10255.0	-801.5
297	DUMMYR5	10325.0	-801.5
298	DUMMYR6	10395.0	-801.5
299	TESTO31	10670.0	796.5
300	TESTO32	10650.0	671.5

R61505 PAD coordinates (Unit: μm) 2005.08.24 rev1.2

pad No	pad name	X	Y
301	DUMMYR7	10630.0	796.5
302	DUMMYR8	10610.0	671.5
303	VGLDMY1	10590.0	796.5
304	G1	10570.0	671.5
305	G3	10550.0	796.5
306	G5	10530.0	671.5
307	G7	10510.0	796.5
308	G9	10490.0	671.5
309	G11	10470.0	796.5
310	G13	10450.0	671.5
311	G15	10430.0	796.5
312	G17	10410.0	671.5
313	G19	10390.0	796.5
314	G21	10370.0	671.5
315	G23	10350.0	796.5
316	G25	10330.0	671.5
317	G27	10310.0	796.5
318	G29	10290.0	671.5
319	G31	10270.0	796.5
320	G33	10250.0	671.5
321	G35	10230.0	796.5
322	G37	10210.0	671.5
323	G39	10190.0	796.5
324	G41	10170.0	671.5
325	G43	10150.0	796.5
326	G45	10130.0	671.5
327	G47	10110.0	796.5
328	G49	10090.0	671.5
329	G51	10070.0	796.5
330	G53	10050.0	671.5
331	G55	10030.0	796.5
332	G57	10010.0	671.5
333	G59	9990.0	796.5
334	G61	9970.0	671.5
335	G63	9950.0	796.5
336	G65	9930.0	671.5
337	G67	9910.0	796.5
338	G69	9890.0	671.5
339	G71	9870.0	796.5
340	G73	9850.0	671.5
341	G75	9830.0	796.5
342	G77	9810.0	671.5
343	G79	9790.0	796.5
344	G81	9770.0	671.5
345	G83	9750.0	796.5
346	G85	9730.0	671.5
347	G87	9710.0	796.5
348	G89	9690.0	671.5
349	G91	9670.0	796.5
350	G93	9650.0	671.5

pad No	pad name	X	Y
351	G95	9630.0	796.5
352	G97	9610.0	671.5
353	G99	9590.0	796.5
354	G101	9570.0	671.5
355	G103	9550.0	796.5
356	G105	9530.0	671.5
357	G107	9510.0	796.5
358	G109	9490.0	671.5
359	G111	9470.0	796.5
360	G113	9450.0	671.5
361	G115	9430.0	796.5
362	G117	9410.0	671.5
363	G119	9390.0	796.5
364	G121	9370.0	671.5
365	G123	9350.0	796.5
366	G125	9330.0	671.5
367	G127	9310.0	796.5
368	G129	9290.0	671.5
369	G131	9270.0	796.5
370	G133	9250.0	671.5
371	G135	9230.0	796.5
372	G137	9210.0	671.5
373	G139	9190.0	796.5
374	G141	9170.0	671.5
375	G143	9150.0	796.5
376	G145	9130.0	671.5
377	G147	9110.0	796.5
378	G149	9090.0	671.5
379	G151	9070.0	796.5
380	G153	9050.0	671.5
381	G155	9030.0	796.5
382	G157	9010.0	671.5
383	G159	8990.0	796.5
384	G161	8970.0	671.5
385	G163	8950.0	796.5
386	G165	8930.0	671.5
387	G167	8910.0	796.5
388	G169	8890.0	671.5
389	G171	8870.0	796.5
390	G173	8850.0	671.5
391	G175	8830.0	796.5
392	G177	8810.0	671.5
393	G179	8790.0	796.5
394	G181	8770.0	671.5
395	G183	8750.0	796.5
396	G185	8730.0	671.5
397	G187	8710.0	796.5
398	G189	8690.0	671.5
399	G191	8670.0	796.5
400	G193	8650.0	671.5

R61505 PAD coordinates (Unit: μm) 2005.08.24 rev1.2

pad No	pad name	X	Y
401	G195	8630.0	796.5
402	G197	8610.0	671.5
403	G199	8590.0	796.5
404	G201	8570.0	671.5
405	G203	8550.0	796.5
406	G205	8530.0	671.5
407	G207	8510.0	796.5
408	G209	8490.0	671.5
409	G211	8470.0	796.5
410	G213	8450.0	671.5
411	G215	8430.0	796.5
412	G217	8410.0	671.5
413	G219	8390.0	796.5
414	G221	8370.0	671.5
415	G223	8350.0	796.5
416	G225	8330.0	671.5
417	G227	8310.0	796.5
418	G229	8290.0	671.5
419	G231	8270.0	796.5
420	G233	8250.0	671.5
421	G235	8230.0	796.5
422	G237	8210.0	671.5
423	G239	8190.0	796.5
424	G241	8170.0	671.5
425	G243	8150.0	796.5
426	G245	8130.0	671.5
427	G247	8110.0	796.5
428	G249	8090.0	671.5
429	G251	8070.0	796.5
430	G253	8050.0	671.5
431	G255	8030.0	796.5
432	G257	8010.0	671.5
433	G259	7990.0	796.5
434	G261	7970.0	671.5
435	G263	7950.0	796.5
436	G265	7930.0	671.5
437	G267	7910.0	796.5
438	G269	7890.0	671.5
439	G271	7870.0	796.5
440	G273	7850.0	671.5
441	G275	7830.0	796.5
442	G277	7810.0	671.5
443	G279	7790.0	796.5
444	G281	7770.0	671.5
445	G283	7750.0	796.5
446	G285	7730.0	671.5
447	G287	7710.0	796.5
448	G289	7690.0	671.5
449	G291	7670.0	796.5
450	G293	7650.0	671.5

pad No	pad name	X	Y
451	G295	7630.0	796.5
452	G297	7610.0	671.5
453	G299	7590.0	796.5
454	G301	7570.0	671.5
455	G303	7550.0	796.5
456	G305	7530.0	671.5
457	G307	7510.0	796.5
458	G309	7490.0	671.5
459	G311	7470.0	796.5
460	G313	7450.0	671.5
461	G315	7430.0	796.5
462	G317	7410.0	671.5
463	G319	7390.0	796.5
464	VGLDMY2	7370.0	671.5
465	TESTO33	7350.0	796.5
466	TESTO34	7130.0	796.5
467	S720	7110.0	671.5
468	S719	7090.0	796.5
469	S718	7070.0	671.5
470	S717	7050.0	796.5
471	S716	7030.0	671.5
472	S715	7010.0	796.5
473	S714	6990.0	671.5
474	S713	6970.0	796.5
475	S712	6950.0	671.5
476	S711	6930.0	796.5
477	S710	6910.0	671.5
478	S709	6890.0	796.5
479	S708	6870.0	671.5
480	S707	6850.0	796.5
481	S706	6830.0	671.5
482	S705	6810.0	796.5
483	S704	6790.0	671.5
484	S703	6770.0	796.5
485	S702	6750.0	671.5
486	S701	6730.0	796.5
487	S700	6710.0	671.5
488	S699	6690.0	796.5
489	S698	6670.0	671.5
490	S697	6650.0	796.5
491	S696	6630.0	671.5
492	S695	6610.0	796.5
493	S694	6590.0	671.5
494	S693	6570.0	796.5
495	S692	6550.0	671.5
496	S691	6530.0	796.5
497	S690	6510.0	671.5
498	S689	6490.0	796.5
499	S688	6470.0	671.5
500	S687	6450.0	796.5

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pad No	pad name	X	Y
501	S686	6430.0	671.5
502	S685	6410.0	796.5
503	S684	6390.0	671.5
504	S683	6370.0	796.5
505	S682	6350.0	671.5
506	S681	6330.0	796.5
507	S680	6310.0	671.5
508	S679	6290.0	796.5
509	S678	6270.0	671.5
510	S677	6250.0	796.5
511	S676	6230.0	671.5
512	S675	6210.0	796.5
513	S674	6190.0	671.5
514	S673	6170.0	796.5
515	S672	6150.0	671.5
516	S671	6130.0	796.5
517	S670	6110.0	671.5
518	S669	6090.0	796.5
519	S668	6070.0	671.5
520	S667	6050.0	796.5
521	S666	6030.0	671.5
522	S665	6010.0	796.5
523	S664	5990.0	671.5
524	S663	5970.0	796.5
525	S662	5950.0	671.5
526	S661	5930.0	796.5
527	S660	5910.0	671.5
528	S659	5890.0	796.5
529	S658	5870.0	671.5
530	S657	5850.0	796.5
531	S656	5830.0	671.5
532	S655	5810.0	796.5
533	S654	5790.0	671.5
534	S653	5770.0	796.5
535	S652	5750.0	671.5
536	S651	5730.0	796.5
537	S650	5710.0	671.5
538	S649	5690.0	796.5
539	S648	5670.0	671.5
540	S647	5650.0	796.5
541	S646	5630.0	671.5
542	S645	5610.0	796.5
543	S644	5590.0	671.5
544	S643	5570.0	796.5
545	S642	5550.0	671.5
546	S641	5530.0	796.5
547	S640	5510.0	671.5
548	S639	5490.0	796.5
549	S638	5470.0	671.5
550	S637	5450.0	796.5

pad No	pad name	X	Y
551	S636	5430.0	671.5
552	S635	5410.0	796.5
553	S634	5390.0	671.5
554	S633	5370.0	796.5
555	S632	5350.0	671.5
556	S631	5330.0	796.5
557	S630	5310.0	671.5
558	S629	5290.0	796.5
559	S628	5270.0	671.5
560	S627	5250.0	796.5
561	S626	5230.0	671.5
562	S625	5210.0	796.5
563	S624	5190.0	671.5
564	S623	5170.0	796.5
565	S622	5150.0	671.5
566	S621	5130.0	796.5
567	S620	5110.0	671.5
568	S619	5090.0	796.5
569	S618	5070.0	671.5
570	S617	5050.0	796.5
571	S616	5030.0	671.5
572	S615	5010.0	796.5
573	S614	4990.0	671.5
574	S613	4970.0	796.5
575	S612	4950.0	671.5
576	S611	4930.0	796.5
577	S610	4910.0	671.5
578	S609	4890.0	796.5
579	S608	4870.0	671.5
580	S607	4850.0	796.5
581	S606	4830.0	671.5
582	S605	4810.0	796.5
583	S604	4790.0	671.5
584	S603	4770.0	796.5
585	S602	4750.0	671.5
586	S601	4730.0	796.5
587	S600	4710.0	671.5
588	S599	4690.0	796.5
589	S598	4670.0	671.5
590	S597	4650.0	796.5
591	S596	4630.0	671.5
592	S595	4610.0	796.5
593	S594	4590.0	671.5
594	S593	4570.0	796.5
595	S592	4550.0	671.5
596	S591	4530.0	796.5
597	S590	4510.0	671.5
598	S589	4490.0	796.5
599	S588	4470.0	671.5
600	S587	4450.0	796.5

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pad No	pad name	X	Y
601	S586	4430.0	671.5
602	S585	4410.0	796.5
603	S584	4390.0	671.5
604	S583	4370.0	796.5
605	S582	4350.0	671.5
606	S581	4330.0	796.5
607	S580	4310.0	671.5
608	S579	4290.0	796.5
609	S578	4270.0	671.5
610	S577	4250.0	796.5
611	S576	4230.0	671.5
612	S575	4210.0	796.5
613	S574	4190.0	671.5
614	S573	4170.0	796.5
615	S572	4150.0	671.5
616	S571	4130.0	796.5
617	S570	4110.0	671.5
618	S569	4090.0	796.5
619	S568	4070.0	671.5
620	S567	4050.0	796.5
621	S566	4030.0	671.5
622	S565	4010.0	796.5
623	S564	3990.0	671.5
624	S563	3970.0	796.5
625	S562	3950.0	671.5
626	S561	3930.0	796.5
627	S560	3910.0	671.5
628	S559	3890.0	796.5
629	S558	3870.0	671.5
630	S557	3850.0	796.5
631	S556	3830.0	671.5
632	S555	3810.0	796.5
633	S554	3790.0	671.5
634	S553	3770.0	796.5
635	S552	3750.0	671.5
636	S551	3730.0	796.5
637	S550	3710.0	671.5
638	S549	3690.0	796.5
639	S548	3670.0	671.5
640	S547	3650.0	796.5
641	S546	3630.0	671.5
642	S545	3610.0	796.5
643	S544	3590.0	671.5
644	S543	3570.0	796.5
645	S542	3550.0	671.5
646	S541	3530.0	796.5
647	S540	3510.0	671.5
648	S539	3490.0	796.5
649	S538	3470.0	671.5
650	S537	3450.0	796.5

pad No	pad name	X	Y
651	S536	3430.0	671.5
652	S535	3410.0	796.5
653	S534	3390.0	671.5
654	S533	3370.0	796.5
655	S532	3350.0	671.5
656	S531	3330.0	796.5
657	S530	3310.0	671.5
658	S529	3290.0	796.5
659	S528	3270.0	671.5
660	S527	3250.0	796.5
661	S526	3230.0	671.5
662	S525	3210.0	796.5
663	S524	3190.0	671.5
664	S523	3170.0	796.5
665	S522	3150.0	671.5
666	S521	3130.0	796.5
667	S520	3110.0	671.5
668	S519	3090.0	796.5
669	S518	3070.0	671.5
670	S517	3050.0	796.5
671	S516	3030.0	671.5
672	S515	3010.0	796.5
673	S514	2990.0	671.5
674	S513	2970.0	796.5
675	S512	2950.0	671.5
676	S511	2930.0	796.5
677	S510	2910.0	671.5
678	S509	2890.0	796.5
679	S508	2870.0	671.5
680	S507	2850.0	796.5
681	S506	2830.0	671.5
682	S505	2810.0	796.5
683	S504	2790.0	671.5
684	S503	2770.0	796.5
685	S502	2750.0	671.5
686	S501	2730.0	796.5
687	S500	2710.0	671.5
688	S499	2690.0	796.5
689	S498	2670.0	671.5
690	S497	2650.0	796.5
691	S496	2630.0	671.5
692	S495	2610.0	796.5
693	S494	2590.0	671.5
694	S493	2570.0	796.5
695	S492	2550.0	671.5
696	S491	2530.0	796.5
697	S490	2510.0	671.5
698	S489	2490.0	796.5
699	S488	2470.0	671.5
700	S487	2450.0	796.5

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pad No	pad name	X	Y
701	S486	2430.0	671.5
702	S485	2410.0	796.5
703	S484	2390.0	671.5
704	S483	2370.0	796.5
705	S482	2350.0	671.5
706	S481	2330.0	796.5
707	S480	2310.0	671.5
708	S479	2290.0	796.5
709	S478	2270.0	671.5
710	S477	2250.0	796.5
711	S476	2230.0	671.5
712	S475	2210.0	796.5
713	S474	2190.0	671.5
714	S473	2170.0	796.5
715	S472	2150.0	671.5
716	S471	2130.0	796.5
717	S470	2110.0	671.5
718	S469	2090.0	796.5
719	S468	2070.0	671.5
720	S467	2050.0	796.5
721	S466	2030.0	671.5
722	S465	2010.0	796.5
723	S464	1990.0	671.5
724	S463	1970.0	796.5
725	S462	1950.0	671.5
726	S461	1930.0	796.5
727	S460	1910.0	671.5
728	S459	1890.0	796.5
729	S458	1870.0	671.5
730	S457	1850.0	796.5
731	S456	1830.0	671.5
732	S455	1810.0	796.5
733	S454	1790.0	671.5
734	S453	1770.0	796.5
735	S452	1750.0	671.5
736	S451	1730.0	796.5
737	S450	1710.0	671.5
738	S449	1690.0	796.5
739	S448	1670.0	671.5
740	S447	1650.0	796.5
741	S446	1630.0	671.5
742	S445	1610.0	796.5
743	S444	1590.0	671.5
744	S443	1570.0	796.5
745	S442	1550.0	671.5
746	S441	1530.0	796.5
747	S440	1510.0	671.5
748	S439	1490.0	796.5
749	S438	1470.0	671.5
750	S437	1450.0	796.5

pad No	pad name	X	Y
751	S436	1430.0	671.5
752	S435	1410.0	796.5
753	S434	1390.0	671.5
754	S433	1370.0	796.5
755	S432	1350.0	671.5
756	S431	1330.0	796.5
757	S430	1310.0	671.5
758	S429	1290.0	796.5
759	S428	1270.0	671.5
760	S427	1250.0	796.5
761	S426	1230.0	671.5
762	S425	1210.0	796.5
763	S424	1190.0	671.5
764	S423	1170.0	796.5
765	S422	1150.0	671.5
766	S421	1130.0	796.5
767	S420	1110.0	671.5
768	S419	1090.0	796.5
769	S418	1070.0	671.5
770	S417	1050.0	796.5
771	S416	1030.0	671.5
772	S415	1010.0	796.5
773	S414	990.0	671.5
774	S413	970.0	796.5
775	S412	950.0	671.5
776	S411	930.0	796.5
777	S410	910.0	671.5
778	S409	890.0	796.5
779	S408	870.0	671.5
780	S407	850.0	796.5
781	S406	830.0	671.5
782	S405	810.0	796.5
783	S404	790.0	671.5
784	S403	770.0	796.5
785	S402	750.0	671.5
786	S401	730.0	796.5
787	S400	710.0	671.5
788	S399	690.0	796.5
789	S398	670.0	671.5
790	S397	650.0	796.5
791	S396	630.0	671.5
792	S395	610.0	796.5
793	S394	590.0	671.5
794	S393	570.0	796.5
795	S392	550.0	671.5
796	S391	530.0	796.5
797	S390	510.0	671.5
798	S389	490.0	796.5
799	S388	470.0	671.5
800	S387	450.0	796.5

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pad No	pad name	X	Y
801	S386	430.0	671.5
802	S385	410.0	796.5
803	S384	390.0	671.5
804	S383	370.0	796.5
805	S382	350.0	671.5
806	S381	330.0	796.5
807	S380	310.0	671.5
808	S379	290.0	796.5
809	S378	270.0	671.5
810	S377	250.0	796.5
811	S376	230.0	671.5
812	S375	210.0	796.5
813	S374	190.0	671.5
814	S373	170.0	796.5
815	S372	150.0	671.5
816	S371	130.0	796.5
817	S370	110.0	671.5
818	S369	90.0	796.5
819	S368	70.0	671.5
820	S367	50.0	796.5
821	S366	30.0	671.5
822	S365	10.0	796.5
823	S364	-10.0	671.5
824	S363	-30.0	796.5
825	S362	-50.0	671.5
826	S361	-70.0	796.5
827	S360	-90.0	671.5
828	S359	-110.0	796.5
829	S358	-130.0	671.5
830	S357	-150.0	796.5
831	S356	-170.0	671.5
832	S355	-190.0	796.5
833	S354	-210.0	671.5
834	S353	-230.0	796.5
835	S352	-250.0	671.5
836	S351	-270.0	796.5
837	S350	-290.0	671.5
838	S349	-310.0	796.5
839	S348	-330.0	671.5
840	S347	-350.0	796.5
841	S346	-370.0	671.5
842	S345	-390.0	796.5
843	S344	-410.0	671.5
844	S343	-430.0	796.5
845	S342	-450.0	671.5
846	S341	-470.0	796.5
847	S340	-490.0	671.5
848	S339	-510.0	796.5
849	S338	-530.0	671.5
850	S337	-550.0	796.5

pad No	pad name	X	Y
851	S336	-570.0	671.5
852	S335	-590.0	796.5
853	S334	-610.0	671.5
854	S333	-630.0	796.5
855	S332	-650.0	671.5
856	S331	-670.0	796.5
857	S330	-690.0	671.5
858	S329	-710.0	796.5
859	S328	-730.0	671.5
860	S327	-750.0	796.5
861	S326	-770.0	671.5
862	S325	-790.0	796.5
863	S324	-810.0	671.5
864	S323	-830.0	796.5
865	S322	-850.0	671.5
866	S321	-870.0	796.5
867	S320	-890.0	671.5
868	S319	-910.0	796.5
869	S318	-930.0	671.5
870	S317	-950.0	796.5
871	S316	-970.0	671.5
872	S315	-990.0	796.5
873	S314	-1010.0	671.5
874	S313	-1030.0	796.5
875	S312	-1050.0	671.5
876	S311	-1070.0	796.5
877	S310	-1090.0	671.5
878	S309	-1110.0	796.5
879	S308	-1130.0	671.5
880	S307	-1150.0	796.5
881	S306	-1170.0	671.5
882	S305	-1190.0	796.5
883	S304	-1210.0	671.5
884	S303	-1230.0	796.5
885	S302	-1250.0	671.5
886	S301	-1270.0	796.5
887	S300	-1290.0	671.5
888	S299	-1310.0	796.5
889	S298	-1330.0	671.5
890	S297	-1350.0	796.5
891	S296	-1370.0	671.5
892	S295	-1390.0	796.5
893	S294	-1410.0	671.5
894	S293	-1430.0	796.5
895	S292	-1450.0	671.5
896	S291	-1470.0	796.5
897	S290	-1490.0	671.5
898	S289	-1510.0	796.5
899	S288	-1530.0	671.5
900	S287	-1550.0	796.5

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pad No	pad name	X	Y
901	S286	-1570.0	671.5
902	S285	-1590.0	796.5
903	S284	-1610.0	671.5
904	S283	-1630.0	796.5
905	S282	-1650.0	671.5
906	S281	-1670.0	796.5
907	S280	-1690.0	671.5
908	S279	-1710.0	796.5
909	S278	-1730.0	671.5
910	S277	-1750.0	796.5
911	S276	-1770.0	671.5
912	S275	-1790.0	796.5
913	S274	-1810.0	671.5
914	S273	-1830.0	796.5
915	S272	-1850.0	671.5
916	S271	-1870.0	796.5
917	S270	-1890.0	671.5
918	S269	-1910.0	796.5
919	S268	-1930.0	671.5
920	S267	-1950.0	796.5
921	S266	-1970.0	671.5
922	S265	-1990.0	796.5
923	S264	-2010.0	671.5
924	S263	-2030.0	796.5
925	S262	-2050.0	671.5
926	S261	-2070.0	796.5
927	S260	-2090.0	671.5
928	S259	-2110.0	796.5
929	S258	-2130.0	671.5
930	S257	-2150.0	796.5
931	S256	-2170.0	671.5
932	S255	-2190.0	796.5
933	S254	-2210.0	671.5
934	S253	-2230.0	796.5
935	S252	-2250.0	671.5
936	S251	-2270.0	796.5
937	S250	-2290.0	671.5
938	S249	-2310.0	796.5
939	S248	-2330.0	671.5
940	S247	-2350.0	796.5
941	S246	-2370.0	671.5
942	S245	-2390.0	796.5
943	S244	-2410.0	671.5
944	S243	-2430.0	796.5
945	S242	-2450.0	671.5
946	S241	-2470.0	796.5
947	S240	-2490.0	671.5
948	S239	-2510.0	796.5
949	S238	-2530.0	671.5
950	S237	-2550.0	796.5

pad No	pad name	X	Y
951	S236	-2570.0	671.5
952	S235	-2590.0	796.5
953	S234	-2610.0	671.5
954	S233	-2630.0	796.5
955	S232	-2650.0	671.5
956	S231	-2670.0	796.5
957	S230	-2690.0	671.5
958	S229	-2710.0	796.5
959	S228	-2730.0	671.5
960	S227	-2750.0	796.5
961	S226	-2770.0	671.5
962	S225	-2790.0	796.5
963	S224	-2810.0	671.5
964	S223	-2830.0	796.5
965	S222	-2850.0	671.5
966	S221	-2870.0	796.5
967	S220	-2890.0	671.5
968	S219	-2910.0	796.5
969	S218	-2930.0	671.5
970	S217	-2950.0	796.5
971	S216	-2970.0	671.5
972	S215	-2990.0	796.5
973	S214	-3010.0	671.5
974	S213	-3030.0	796.5
975	S212	-3050.0	671.5
976	S211	-3070.0	796.5
977	S210	-3090.0	671.5
978	S209	-3110.0	796.5
979	S208	-3130.0	671.5
980	S207	-3150.0	796.5
981	S206	-3170.0	671.5
982	S205	-3190.0	796.5
983	S204	-3210.0	671.5
984	S203	-3230.0	796.5
985	S202	-3250.0	671.5
986	S201	-3270.0	796.5
987	S200	-3290.0	671.5
988	S199	-3310.0	796.5
989	S198	-3330.0	671.5
990	S197	-3350.0	796.5
991	S196	-3370.0	671.5
992	S195	-3390.0	796.5
993	S194	-3410.0	671.5
994	S193	-3430.0	796.5
995	S192	-3450.0	671.5
996	S191	-3470.0	796.5
997	S190	-3490.0	671.5
998	S189	-3510.0	796.5
999	S188	-3530.0	671.5
1000	S187	-3550.0	796.5

R61505 PAD coordinates (Unit: μm) 2005.08.24 rev1.2

pad No	pad name	X	Y
1001	S186	-3570.0	671.5
1002	S185	-3590.0	796.5
1003	S184	-3610.0	671.5
1004	S183	-3630.0	796.5
1005	S182	-3650.0	671.5
1006	S181	-3670.0	796.5
1007	S180	-3690.0	671.5
1008	S179	-3710.0	796.5
1009	S178	-3730.0	671.5
1010	S177	-3750.0	796.5
1011	S176	-3770.0	671.5
1012	S175	-3790.0	796.5
1013	S174	-3810.0	671.5
1014	S173	-3830.0	796.5
1015	S172	-3850.0	671.5
1016	S171	-3870.0	796.5
1017	S170	-3890.0	671.5
1018	S169	-3910.0	796.5
1019	S168	-3930.0	671.5
1020	S167	-3950.0	796.5
1021	S166	-3970.0	671.5
1022	S165	-3990.0	796.5
1023	S164	-4010.0	671.5
1024	S163	-4030.0	796.5
1025	S162	-4050.0	671.5
1026	S161	-4070.0	796.5
1027	S160	-4090.0	671.5
1028	S159	-4110.0	796.5
1029	S158	-4130.0	671.5
1030	S157	-4150.0	796.5
1031	S156	-4170.0	671.5
1032	S155	-4190.0	796.5
1033	S154	-4210.0	671.5
1034	S153	-4230.0	796.5
1035	S152	-4250.0	671.5
1036	S151	-4270.0	796.5
1037	S150	-4290.0	671.5
1038	S149	-4310.0	796.5
1039	S148	-4330.0	671.5
1040	S147	-4350.0	796.5
1041	S146	-4370.0	671.5
1042	S145	-4390.0	796.5
1043	S144	-4410.0	671.5
1044	S143	-4430.0	796.5
1045	S142	-4450.0	671.5
1046	S141	-4470.0	796.5
1047	S140	-4490.0	671.5
1048	S139	-4510.0	796.5
1049	S138	-4530.0	671.5
1050	S137	-4550.0	796.5

pad No	pad name	X	Y
1051	S136	-4570.0	671.5
1052	S135	-4590.0	796.5
1053	S134	-4610.0	671.5
1054	S133	-4630.0	796.5
1055	S132	-4650.0	671.5
1056	S131	-4670.0	796.5
1057	S130	-4690.0	671.5
1058	S129	-4710.0	796.5
1059	S128	-4730.0	671.5
1060	S127	-4750.0	796.5
1061	S126	-4770.0	671.5
1062	S125	-4790.0	796.5
1063	S124	-4810.0	671.5
1064	S123	-4830.0	796.5
1065	S122	-4850.0	671.5
1066	S121	-4870.0	796.5
1067	S120	-4890.0	671.5
1068	S119	-4910.0	796.5
1069	S118	-4930.0	671.5
1070	S117	-4950.0	796.5
1071	S116	-4970.0	671.5
1072	S115	-4990.0	796.5
1073	S114	-5010.0	671.5
1074	S113	-5030.0	796.5
1075	S112	-5050.0	671.5
1076	S111	-5070.0	796.5
1077	S110	-5090.0	671.5
1078	S109	-5110.0	796.5
1079	S108	-5130.0	671.5
1080	S107	-5150.0	796.5
1081	S106	-5170.0	671.5
1082	S105	-5190.0	796.5
1083	S104	-5210.0	671.5
1084	S103	-5230.0	796.5
1085	S102	-5250.0	671.5
1086	S101	-5270.0	796.5
1087	S100	-5290.0	671.5
1088	S99	-5310.0	796.5
1089	S98	-5330.0	671.5
1090	S97	-5350.0	796.5
1091	S96	-5370.0	671.5
1092	S95	-5390.0	796.5
1093	S94	-5410.0	671.5
1094	S93	-5430.0	796.5
1095	S92	-5450.0	671.5
1096	S91	-5470.0	796.5
1097	S90	-5490.0	671.5
1098	S89	-5510.0	796.5
1099	S88	-5530.0	671.5
1100	S87	-5550.0	796.5

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pad No	pad name	X	Y
1101	S86	-5570.0	671.5
1102	S85	-5590.0	796.5
1103	S84	-5610.0	671.5
1104	S83	-5630.0	796.5
1105	S82	-5650.0	671.5
1106	S81	-5670.0	796.5
1107	S80	-5690.0	671.5
1108	S79	-5710.0	796.5
1109	S78	-5730.0	671.5
1110	S77	-5750.0	796.5
1111	S76	-5770.0	671.5
1112	S75	-5790.0	796.5
1113	S74	-5810.0	671.5
1114	S73	-5830.0	796.5
1115	S72	-5850.0	671.5
1116	S71	-5870.0	796.5
1117	S70	-5890.0	671.5
1118	S69	-5910.0	796.5
1119	S68	-5930.0	671.5
1120	S67	-5950.0	796.5
1121	S66	-5970.0	671.5
1122	S65	-5990.0	796.5
1123	S64	-6010.0	671.5
1124	S63	-6030.0	796.5
1125	S62	-6050.0	671.5
1126	S61	-6070.0	796.5
1127	S60	-6090.0	671.5
1128	S59	-6110.0	796.5
1129	S58	-6130.0	671.5
1130	S57	-6150.0	796.5
1131	S56	-6170.0	671.5
1132	S55	-6190.0	796.5
1133	S54	-6210.0	671.5
1134	S53	-6230.0	796.5
1135	S52	-6250.0	671.5
1136	S51	-6270.0	796.5
1137	S50	-6290.0	671.5
1138	S49	-6310.0	796.5
1139	S48	-6330.0	671.5
1140	S47	-6350.0	796.5
1141	S46	-6370.0	671.5
1142	S45	-6390.0	796.5
1143	S44	-6410.0	671.5
1144	S43	-6430.0	796.5
1145	S42	-6450.0	671.5
1146	S41	-6470.0	796.5
1147	S40	-6490.0	671.5
1148	S39	-6510.0	796.5
1149	S38	-6530.0	671.5
1150	S37	-6550.0	796.5

pad No	pad name	X	Y
1151	S36	-6570.0	671.5
1152	S35	-6590.0	796.5
1153	S34	-6610.0	671.5
1154	S33	-6630.0	796.5
1155	S32	-6650.0	671.5
1156	S31	-6670.0	796.5
1157	S30	-6690.0	671.5
1158	S29	-6710.0	796.5
1159	S28	-6730.0	671.5
1160	S27	-6750.0	796.5
1161	S26	-6770.0	671.5
1162	S25	-6790.0	796.5
1163	S24	-6810.0	671.5
1164	S23	-6830.0	796.5
1165	S22	-6850.0	671.5
1166	S21	-6870.0	796.5
1167	S20	-6890.0	671.5
1168	S19	-6910.0	796.5
1169	S18	-6930.0	671.5
1170	S17	-6950.0	796.5
1171	S16	-6970.0	671.5
1172	S15	-6990.0	796.5
1173	S14	-7010.0	671.5
1174	S13	-7030.0	796.5
1175	S12	-7050.0	671.5
1176	S11	-7070.0	796.5
1177	S10	-7090.0	671.5
1178	S9	-7110.0	796.5
1179	S8	-7130.0	671.5
1180	S7	-7150.0	796.5
1181	S6	-7170.0	671.5
1182	S5	-7190.0	796.5
1183	S4	-7210.0	671.5
1184	S3	-7230.0	796.5
1185	S2	-7250.0	671.5
1186	S1	-7270.0	796.5
1187	TESTO35	-7290.0	671.5
1188	TESTO36	-7350.0	796.5
1189	VGLDMY3	-7370.0	671.5
1190	G320	-7390.0	796.5
1191	G318	-7410.0	671.5
1192	G316	-7430.0	796.5
1193	G314	-7450.0	671.5
1194	G312	-7470.0	796.5
1195	G310	-7490.0	671.5
1196	G308	-7510.0	796.5
1197	G306	-7530.0	671.5
1198	G304	-7550.0	796.5
1199	G302	-7570.0	671.5
1200	G300	-7590.0	796.5

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pad No	pad name	X	Y
1201	G298	-7610.0	671.5
1202	G296	-7630.0	796.5
1203	G294	-7650.0	671.5
1204	G292	-7670.0	796.5
1205	G290	-7690.0	671.5
1206	G288	-7710.0	796.5
1207	G286	-7730.0	671.5
1208	G284	-7750.0	796.5
1209	G282	-7770.0	671.5
1210	G280	-7790.0	796.5
1211	G278	-7810.0	671.5
1212	G276	-7830.0	796.5
1213	G274	-7850.0	671.5
1214	G272	-7870.0	796.5
1215	G270	-7890.0	671.5
1216	G268	-7910.0	796.5
1217	G266	-7930.0	671.5
1218	G264	-7950.0	796.5
1219	G262	-7970.0	671.5
1220	G260	-7990.0	796.5
1221	G258	-8010.0	671.5
1222	G256	-8030.0	796.5
1223	G254	-8050.0	671.5
1224	G252	-8070.0	796.5
1225	G250	-8090.0	671.5
1226	G248	-8110.0	796.5
1227	G246	-8130.0	671.5
1228	G244	-8150.0	796.5
1229	G242	-8170.0	671.5
1230	G240	-8190.0	796.5
1231	G238	-8210.0	671.5
1232	G236	-8230.0	796.5
1233	G234	-8250.0	671.5
1234	G232	-8270.0	796.5
1235	G230	-8290.0	671.5
1236	G228	-8310.0	796.5
1237	G226	-8330.0	671.5
1238	G224	-8350.0	796.5
1239	G222	-8370.0	671.5
1240	G220	-8390.0	796.5
1241	G218	-8410.0	671.5
1242	G216	-8430.0	796.5
1243	G214	-8450.0	671.5
1244	G212	-8470.0	796.5
1245	G210	-8490.0	671.5
1246	G208	-8510.0	796.5
1247	G206	-8530.0	671.5
1248	G204	-8550.0	796.5
1249	G202	-8570.0	671.5
1250	G200	-8590.0	796.5

pad No	pad name	X	Y
1251	G198	-8610.0	671.5
1252	G196	-8630.0	796.5
1253	G194	-8650.0	671.5
1254	G192	-8670.0	796.5
1255	G190	-8690.0	671.5
1256	G188	-8710.0	796.5
1257	G186	-8730.0	671.5
1258	G184	-8750.0	796.5
1259	G182	-8770.0	671.5
1260	G180	-8790.0	796.5
1261	G178	-8810.0	671.5
1262	G176	-8830.0	796.5
1263	G174	-8850.0	671.5
1264	G172	-8870.0	796.5
1265	G170	-8890.0	671.5
1266	G168	-8910.0	796.5
1267	G166	-8930.0	671.5
1268	G164	-8950.0	796.5
1269	G162	-8970.0	671.5
1270	G160	-8990.0	796.5
1271	G158	-9010.0	671.5
1272	G156	-9030.0	796.5
1273	G154	-9050.0	671.5
1274	G152	-9070.0	796.5
1275	G150	-9090.0	671.5
1276	G148	-9110.0	796.5
1277	G146	-9130.0	671.5
1278	G144	-9150.0	796.5
1279	G142	-9170.0	671.5
1280	G140	-9190.0	796.5
1281	G138	-9210.0	671.5
1282	G136	-9230.0	796.5
1283	G134	-9250.0	671.5
1284	G132	-9270.0	796.5
1285	G130	-9290.0	671.5
1286	G128	-9310.0	796.5
1287	G126	-9330.0	671.5
1288	G124	-9350.0	796.5
1289	G122	-9370.0	671.5
1290	G120	-9390.0	796.5
1291	G118	-9410.0	671.5
1292	G116	-9430.0	796.5
1293	G114	-9450.0	671.5
1294	G112	-9470.0	796.5
1295	G110	-9490.0	671.5
1296	G108	-9510.0	796.5
1297	G106	-9530.0	671.5
1298	G104	-9550.0	796.5
1299	G102	-9570.0	671.5
1300	G100	-9590.0	796.5

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pad No	pad name	X	Y
1301	G98	-9610.0	671.5
1302	G96	-9630.0	796.5
1303	G94	-9650.0	671.5
1304	G92	-9670.0	796.5
1305	G90	-9690.0	671.5
1306	G88	-9710.0	796.5
1307	G86	-9730.0	671.5
1308	G84	-9750.0	796.5
1309	G82	-9770.0	671.5
1310	G80	-9790.0	796.5
1311	G78	-9810.0	671.5
1312	G76	-9830.0	796.5
1313	G74	-9850.0	671.5
1314	G72	-9870.0	796.5
1315	G70	-9890.0	671.5
1316	G68	-9910.0	796.5
1317	G66	-9930.0	671.5
1318	G64	-9950.0	796.5
1319	G62	-9970.0	671.5
1320	G60	-9990.0	796.5
1321	G58	-10010.0	671.5
1322	G56	-10030.0	796.5
1323	G54	-10050.0	671.5
1324	G52	-10070.0	796.5
1325	G50	-10090.0	671.5
1326	G48	-10110.0	796.5
1327	G46	-10130.0	671.5
1328	G44	-10150.0	796.5
1329	G42	-10170.0	671.5
1330	G40	-10190.0	796.5
1331	G38	-10210.0	671.5
1332	G36	-10230.0	796.5
1333	G34	-10250.0	671.5
1334	G32	-10270.0	796.5
1335	G30	-10290.0	671.5
1336	G28	-10310.0	796.5
1337	G26	-10330.0	671.5
1338	G24	-10350.0	796.5
1339	G22	-10370.0	671.5
1340	G20	-10390.0	796.5
1341	G18	-10410.0	671.5
1342	G16	-10430.0	796.5
1343	G14	-10450.0	671.5
1344	G12	-10470.0	796.5
1345	G10	-10490.0	671.5
1346	G8	-10510.0	796.5
1347	G6	-10530.0	671.5
1348	G4	-10550.0	796.5
1349	G2	-10570.0	671.5
1350	VGLDMY4	-10590.0	796.5

pad No	pad name	X	Y
1351	DUMMYR9	-10610.0	671.5
1352	DUMMYR10	-10630.0	796.5
1353	TESTO37	-10650.0	671.5
1354	TESTO38	-10670.0	796.5

Alignment mark	X	Y
1-a	-10613.0	-753.0
1-b	10613.0	-753.0
2-a	-10572.0	-613.0
2-b	10572.0	-613.0
5-a	-10613.0	-285.8
5-b	10613.0	-285.8

BUMP Arrangement

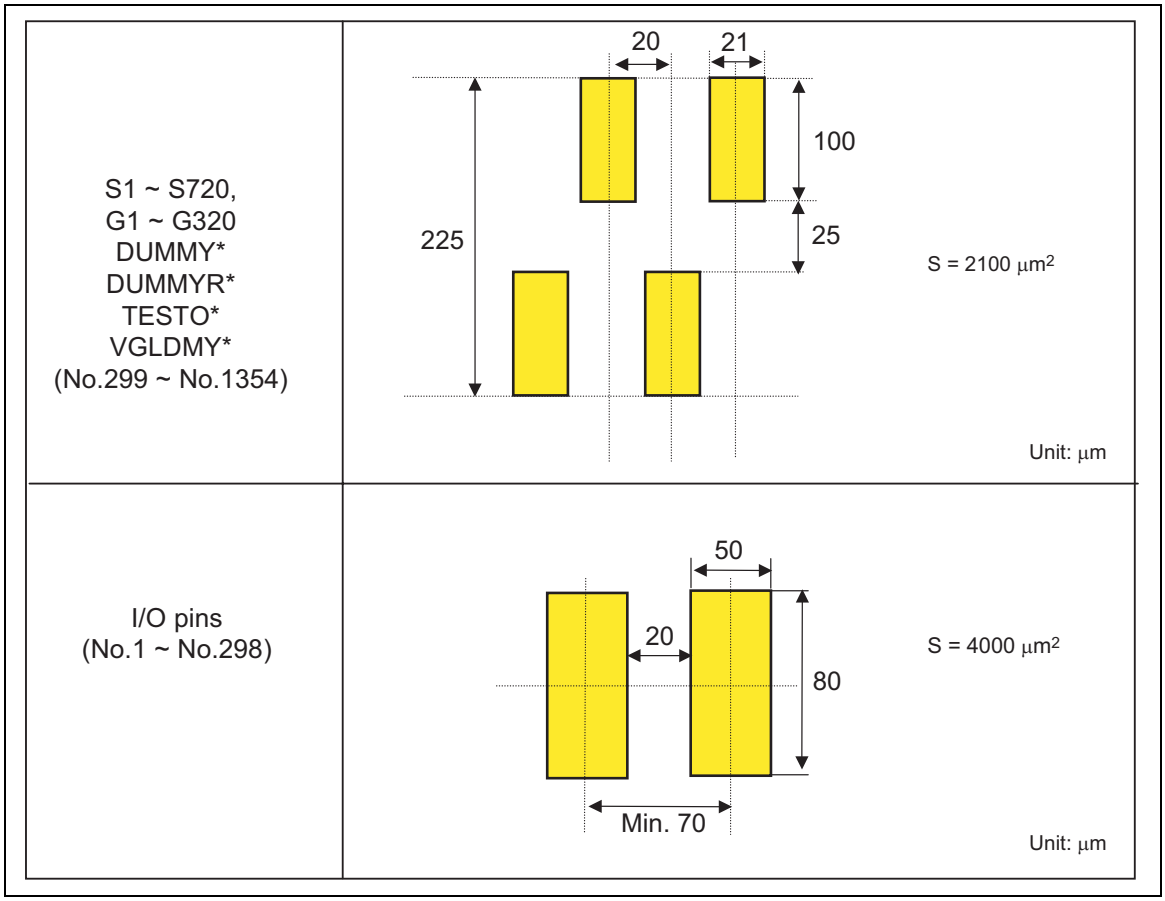

Figure 2

R61505 Recommended connection example and resistance

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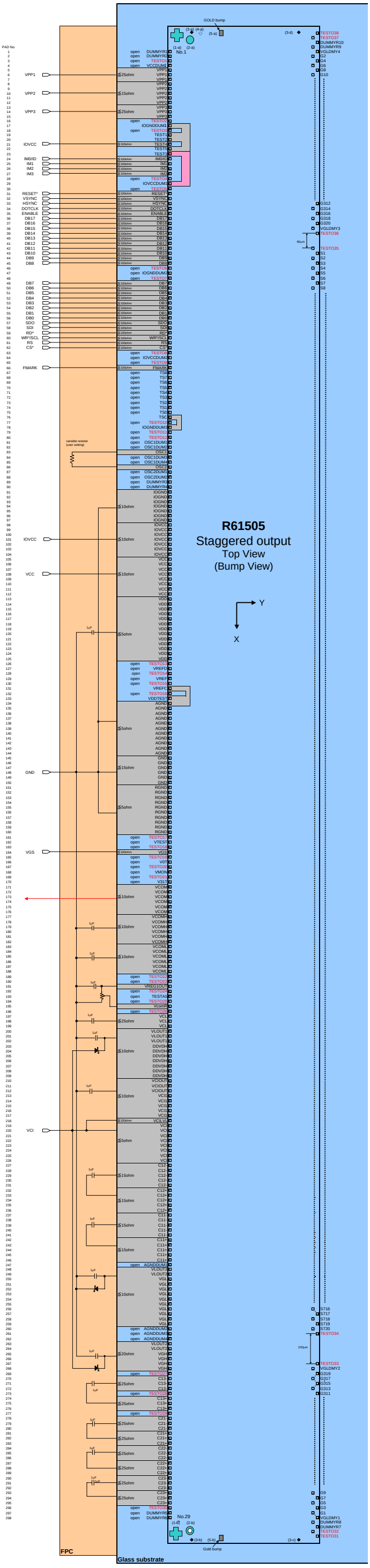


Note: The wiring resistance is a recommended value and it is desirable to set the resistance as small as possible.

GRAM Address Map

Table 6 GRAM Address and Display Position on the Panel (SS = 0, BGR = 0)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			.....	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G320	h00000			h00001			h00002			h00003			.....	h000EC			h000ED			h000EE			h000EF		
G2	G319	h00100			h00101			h00102			h00103			.....	h001EC			h001ED			h001EE			h001EF		
G3	G318	h00200			h00201			h00202			h00203			.....	h002EC			h002ED			h002EE			h002EF		
G4	G317	h00300			h00301			h00302			h00303			.....	h003EC			h003ED			h003EE			h003EF		
G5	G316	h00400			h00401			h00402			h00403			.....	h004EC			h004ED			h004EE			h004EF		
G6	G315	h00500			h00501			h00502			h00503			.....	h005EC			h005ED			h005EE			h005EF		
G7	G314	h00600			h00601			h00602			h00603			.....	h006EC			h006ED			h006EE			h006EF		
G8	G313	h00700			h00701			h00702			h00703			.....	h007EC			h007ED			h007EE			h007EF		
G9	G312	h00800			h00801			h00802			h00803			.....	h008EC			h008ED			h008EE			h008EF		
G10	G311	h00900			h00901			h00902			h00903			.....	h009EC			h009ED			h009EE			h009EF		
G11	G310	h00A00			h00A01			h00A02			h00A03			.....	h00AEC			h00AED			h00AEE			h00AEF		
G12	G309	h00B00			h00B01			h00B02			h00B03			.....	h00BEC			h00BED			h00BEE			h00BEF		
G13	G308	h00C00			h00C01			h00C02			h00C03			.....	h00CEC			h00CED			h00CEE			h00CEF		
G14	G307	h00D00			h00D01			h00D02			h00D03			.....	h00DEC			h00DED			h00DEE			h00DEF		
G15	G306	h00E00			h00E01			h00E02			h00E03			.....	h00EEC			h00EED			h00EEE			h00EEF		
G16	G305	h00F00			h00F01			h00F02			h00F03			.....	h00FEC			h00FED			h00FEE			h00FEF		
G17	G304	h01000			h01001			h01002			h01003			.....	h010EC			h010ED			h010EE			h010EF		
G18	G303	h01100			h01101			h01102			h01103			.....	h011EC			h011ED			h011EE			h011EF		
G19	G302	h01200			h01201			h01202			h01203			.....	h012EC			h012ED			h012EE			h012EF		
G20	G301	h01300			h01301			h01302			h01303			.....	h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:			:	:			:			:			:		
G305	G16	h13000			h13001			h13002			h13003			.....	h130EC			h130ED			h130EE			h130EF		
G306	G15	h13100			h13101			h13102			h13103			.....	h131EC			h131ED			h131EE			h131EF		
G307	G14	h13200			h13201			h13202			h13203			.....	h132EC			h132ED			h132EE			h132EF		
G308	G13	h13300			h13301			h13302			h13303			.....	h133EC			h133ED			h133EE			h133EF		
G309	G12	h13400			h13401			h13402			h13403			.....	h134EC			h134ED			h134EE			h134EF		
G310	G11	h13500			h13501			h13502			h13503			.....	h135EC			h135ED			h135EE			h135EF		
G311	G10	h13600			h13601			h13602			h13603			.....	h136EC			h136ED			h136EE			h136EF		
G312	G9	h13700			h13701			h13702			h13703			.....	h137EC			h137ED			h137EE			h137EF		
G313	G8	h13800			h13801			h13802			h13803			.....	h138EC			h138ED			h138EE			h138EF		
G314	G7	h13900			h13901			h13902			h13903			.....	h139EC			h139ED			h139EE			h139EF		
G315	G6	h13A00			h13A01			h13A02			h13A03			.....	h13AEC			h13AED			h13AEE			h13AEF		
G316	G5	h13B00			h13B01			h13B02			h13B03			.....	h13BEC			h13BED			h13BEE			h13BEF		
G317	G4	h13C00			h13C01			h13C02			h13C03			.....	h13CEC			h13CED			h13CEE			h13CEF		
G318	G3	h13D00			h13D01			h13D02			h13D03			.....	h13DEC			h13DED			h13DEE			h13DEF		
G319	G2	h13E00			h13E01			h13E02			h13E03			.....	h13EEC			h13EED			h13EEE			h13EEF		
G320	G1	h13F00			h13F01			h13F02			h13F03			.....	h13FEC			h13FED			h13FEE			h13FEF		

Table 7 GRAM Address and Display Position on the Panel (SS = 1, BGR = 1)

S/G pin		S720	S719	S718	S717	S716	S715	S714	S713	S712	S711	S710	S709	.....	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			.....	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G320	h00000			h00001			h00002			h00003			.....	h000EC			h000ED			h000EE			h000EF		
G2	G319	h00100			h00101			h00102			h00103			.....	h001EC			h001ED			h001EE			h001EF		
G3	G318	h00200			h00201			h00202			h00203			.....	h002EC			h002ED			h002EE			h002EF		
G4	G317	h00300			h00301			h00302			h00303			.....	h003EC			h003ED			h003EE			h003EF		
G5	G316	h00400			h00401			h00402			h00403			.....	h004EC			h004ED			h004EE			h004EF		
G6	G315	h00500			h00501			h00502			h00503			.....	h005EC			h005ED			h005EE			h005EF		
G7	G314	h00600			h00601			h00602			h00603			.....	h006EC			h006ED			h006EE			h006EF		
G8	G313	h00700			h00701			h00702			h00703			.....	h007EC			h007ED			h007EE			h007EF		
G9	G312	h00800			h00801			h00802			h00803			.....	h008EC			h008ED			h008EE			h008EF		
G10	G311	h00900			h00901			h00902			h00903			.....	h009EC			h009ED			h009EE			h009EF		
G11	G310	h00A00			h00A01			h00A02			h00A03			.....	h00AEC			h00AED			h00AEE			h00AEF		
G12	G309	h00B00			h00B01			h00B02			h00B03			.....	h00BEC			h00BED			h00BEE			h00BEF		
G13	G308	h00C00			h00C01			h00C02			h00C03			.....	h00CEC			h00CED			h00CEE			h00CEF		
G14	G307	h00D00			h00D01			h00D02			h00D03			.....	h00DEC			h00DED			h00DEE			h00DEF		
G15	G306	h00E00			h00E01			h00E02			h00E03			.....	h00EEC			h00EED			h00EEE			h00EEF		
G16	G305	h00F00			h00F01			h00F02			h00F03			.....	h00FEC			h00FED			h00FEE			h00FEF		
G17	G304	h01000			h01001			h01002			h01003			.....	h010EC			h010ED			h010EE			h010EF		
G18	G303	h01100			h01101			h01102			h01103			.....	h011EC			h011ED			h011EE			h011EF		
G19	G302	h01200			h01201			h01202			h01203			.....	h012EC			h012ED			h012EE			h012EF		
G20	G301	h01300			h01301			h01302			h01303			.....	h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:			:	:			:			:			:		
G305	G16	h13000			h13001			h13002			h13003			.....	h130EC			h130ED			h130EE			h130EF		
G306	G15	h13100			h13101			h13102			h13103			.....	h131EC			h131ED			h131EE			h131EF		
G307	G14	h13200			h13201			h13202			h13203			.....	h132EC			h132ED			h132EE			h132EF		
G308	G13	h13300			h13301			h13302			h13303			.....	h133EC			h133ED			h133EE			h133EF		
G309	G12	h13400			h13401			h13402			h13403			.....	h134EC			h134ED			h134EE			h134EF		
G310	G11	h13500			h13501			h13502			h13503			.....	h135EC			h135ED			h135EE			h135EF		
G311	G10	h13600			h13601			h13602			h13603			.....	h136EC			h136ED			h136EE			h136EF		
G312	G9	h13700			h13701			h13702			h13703			.....	h137EC			h137ED			h137EE			h137EF		
G313	G8	h13800			h13801			h13802			h13803			.....	h138EC			h138ED			h138EE			h138EF		
G314	G7	h13900			h13901			h13902			h13903			.....	h139EC			h139ED			h139EE			h139EF		
G315	G6	h13A00			h13A01			h13A02			h13A03			.....	h13AEC			h13AED			h13AEE			h13AEF		
G316	G5	h13B00			h13B01			h13B02			h13B03			.....	h13BEC			h13BED			h13BEE			h13BEF		
G317	G4	h13C00			h13C01			h13C02			h13C03			.....	h13CEC			h13CED			h13CEE			h13CEF		
G318	G3	h13D00			h13D01			h13D02			h13D03			.....	h13DEC			h13DED			h13DEE			h13DEF		
G319	G2	h13E00			h13E01			h13E02			h13E03			.....	h13EEC			h13EED			h13EEE			h13EEF		
G320	G1	h13F00			h13F01			h13F02			h13F03			.....	h13FEC			h13FED			h13FEE			h13FEF		

Instruction

Outline

The R61505 adopts 18-bit bus architecture in order to interface to high-performance microcomputer in high speed. The R61505 starts internal processing after storing control information of externally sent data (16, 8, 1 bit(s)) in the instruction register (IR) and the data register (DR). Since the internal operation of the R61505 is controlled by the signals sent from the microcomputer, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 ~ IB0) are called instruction. When accessing the R61505's internal RAM, data is processed in units of 18 bits. The following are the kinds of instruction of the R61505.

1. Specify index
2. Display control
3. Power management control
4. Set internal GRAM address
5. Transfer data to and from the internal GRAM
6. γ-correction
7. Window address control
8. Screen Display Control

Normally, the instruction to write data is used the most often. The internal GRAM address is updated automatically as data is written to the internal GRAM, which, in combination with the window address function, contributes to minimizing data transfer and thereby lessens the load on the microcomputer. The R61505 writes instructions consecutively by executing the instruction within the cycle when it is written (instruction execution time: 0 cycle).

Instruction Data Format

As the following figure shows, the data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface.

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface.

Write 0 or 1 to the instruction bit to which no instruction is allocated, following the figures of registers. When some of the instruction bit settings are changed, the setting should be made for the instruction bits that the settings are not changed in the same index.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	ID [10]	ID [9]	ID [8]	ID [7]	ID [6]	ID [5]	ID [4]	ID [3]	ID [2]	ID [1]	ID [0]

The index register specifies the index R00h to RFFh of the control register or RAM control to be accessed using a binary number from “0000_0000” to “1111_1111”. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

Display Control

Device Code Read (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1

The device code “1505”H is read out when reading out this register forcibly.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = "0", the source driver output shift from S1 to S720.
When SS = "1", the source driver output shift from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = "0" and BGR = "0", RGB dots are assigned one to one from S1 to S720.
When SS = "1" and BGR = "1", RGB dots are assigned one to one from S720 to S1.

When changing the SS and BGR bits, RAM data must be rewritten.

SM: Controls the scan mode in combination with GS setting. See " Scan mode setting".

LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

BC0: Selects the liquid crystal drive waveform VCOM. See "Line Inversion AC Drive" for details.

B/C = 0: frame inversion waveform is selected.
B/C = 1: line inversion waveform is selected when EOR = 1.

In either liquid crystal drive method, the polarity inversion is halted in blank period (back and front porch periods).

EOR: Enables liquid-crystal line-inversion drive when EOR = 1 and BC0 = 1

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRIREG	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D [1]	I/D [0]	AM	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

The entry mode register includes instruction bits for setting how to write data from the microcomputer to the internal GRAM of the R61505.

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the R61505 writes data to the internal GRAM.

AM = "0", sets the horizontal direction.
AM = "1", sets the vertical direction.

When making a window address area, the data is written only within the area in the direction determined by I/D1-0, AM bits.

I/D[1:0]: Either increments (+1) or decrements (-1) the address counter (AC) automatically as the data is written to the GRAM. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]). The AM bit sets either horizontal or vertical direction in updating RAM address counter automatically when writing data to the internal RAM.

ORG: Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data within the window address area using high-speed RAM write function. Also see Figure 3 and Figure 4.

ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.
ORG = 1: The origin address "h00000" is moved according to the I/D[1:0] setting.

Notes: 1. When ORG = 1, only the origin address "h00000" can be set in the RAM address set registers (R20h, R21h).
2. In RAM read operation, make sure to set ORG = 0.

HWM: The R61505 writes data in high speed with low power consumption by setting HWM = 1. The data to be written within the window address area is buffered in order to write the data in units of horizontal lines. This can minimize the number of RAM access and the power consumption required in data write operation.

When HWM = 1, make sure to set AM = 0 (horizontal direction) and write the data in each horizontal line of the window address area at a time. If the data is not enough to rewrite the horizontal line of the window address area, the GRAM data in that line is not overwritten.

Notes: 1. The R61505 requires no dummy write operation in high-speed write operation.
2. When terminating RAM data write operation in the middle of the line and executing another instruction, the data in the buffer is cleared.

3. When switching from high-speed RAM write operation to index write operation, wait at least 2 normal-write cycle periods (2 t_{cycw} periods).

BGR: Reverses the order from RGB to BGR in writing 18-bit pixel data in the GRAM.

BGR = 0: Write data in the order of RGB to the GRAM.
BGR = 1: Reverse the order from RGB to BGR in writing data to the GRAM.

BGR = 0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR = 1

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

DFM: In combination with the TRIREG setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM = 0 when not transferring data via 16-bit or 8-bit interface.

TRIREG: Selects the format to transfer data bits via 16-bit or 8-bit interface.

In 8-bit interface operation,
TRIREG = 0: 16-bit RAM data is transferred in two transfers.
TRIREG = 1: 18-bit RAM data is transferred in three transfers.

In 16-bit bus interface operation,
TRIREG = 0: 16-bit RAM data is transferred in one transfer.
TRIREG = 1: 18-bit RAM data is transferred in two transfers.

Make sure TRIREG = 0 when not transferring data via 16-bit or 8-bit interface. Also, set TRIREG = 0 during read operation.

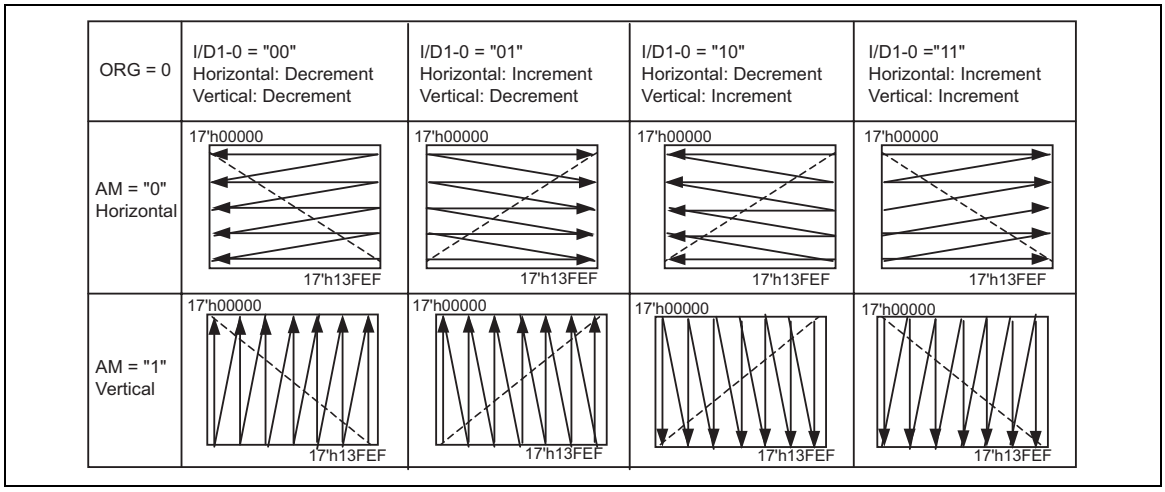


Figure 3 Automatic Address Update (ORG = 0, AM, ID)

Note: When writing data within the window address area with ORG = 0, any address within the window address area can be designated as the starting point of RAM write operation.

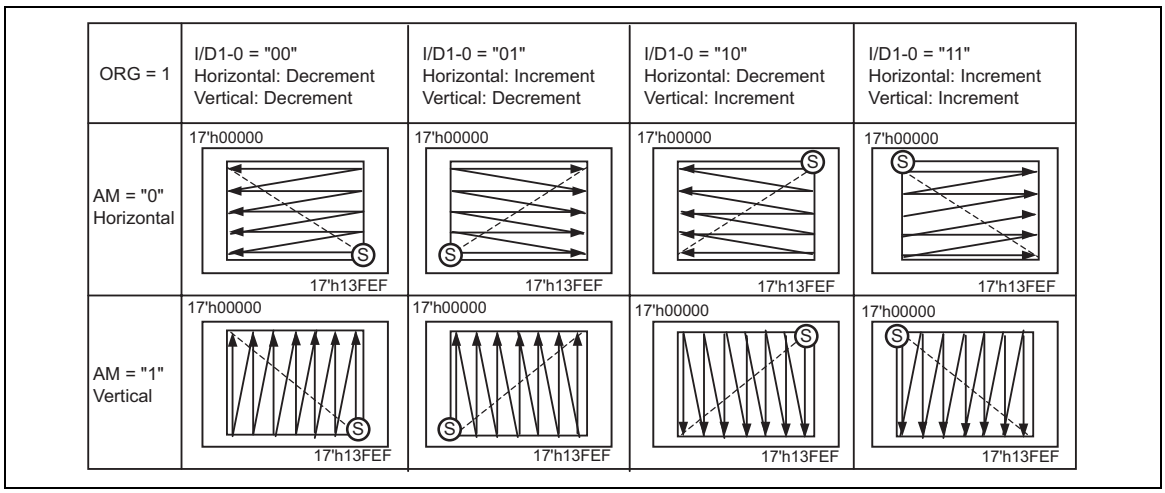


Figure 4 Automatic Address Update (ORG = 1, AM, ID)

Notes: 1. When ORG = 1, make sure to set the address "h00000" in the RAM address set registers (R210h, R21h). Setting other addresses is inhibited.

2. When ORG = 1, the starting point of writing data within the window address area can be set at either corner of the window address area ("S" in circle in the above figure).

Resizing Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV [1]	RCV [0]	0	0	RCH [1]	RCH [0]	0	0	RSZ [1]	RSZ [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSZ[1:0]: Sets the resizing factor. When the RSZ bits are set for resizing, the R61505 writes the data according to the resizing factor so that the original image is displayed in horizontal and vertical dimensions contracted according to the factor . See "Resizing Function".

RCH[1:0]: Sets the number of pixels made as the remainder in horizontal direction when resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

RCV[1:0]: Sets the number of pixels made as the remainder in vertical direction when resizing a picture. By specifying the number of remainder pixels with the RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

Table 8 Resizing Factor (RSR)

RSR [1:0]	Resizing Scale
2'h0	No resizing (x1)
2'h1	x 1/2
2'h2	Setting inhibited
2'h3	x 1/4

Table 9 Remainder Pixels in Horizontal Direction (RCH)

RCH [1:0]	Number of Remainder Pixels in Horizontal Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Note: 1 pixel = 1RGB

Table 10 Remainder Pixels in Vertical Direction (RCV)

RCV [1:0]	Number of Remainder Pixels in Vertical Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Note: 1 pixel = 1RGB

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTDE [1]	PTDE [0]	0	0	0	BASE E	0	VON	GON	DTE	COL	0	D [1]	D [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0]: A graphics display is turned on the screen when writing D1 = "1", and is turned off when writing D1 = "0". When writing D1 = "0", the graphics display data is retained in the internal GRAM and the R61505 displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D1-0 = 2'b01, the R61505 continues internal display operation. When the display is turned off by setting D1-0 = 2'b00, the R61505's internal display operation is halted completely. In combination with the GON setting, the D[1:0] setting controls display ON/OFF. For details, see "Instruction Setting".

Table 11 Source Output Level and Display Operation

D[1:0]	BASEE	Source Output (S1-240)	FMARK Signal	Internal Operation
2'h0	*	GND	Halt	Halt
2'h1	*	GND	Operation	Operation
2'h2	*	Non-lit display	Operation	Operation
2'h3	0	Non-lit display	Operation	Operation
	1	Base-image display	Operation	Operation

Notes: 1: The data write operation from the microcomputer is not affected by the D[1:0] setting.
2: The PTS bits set the source output level for "Non-lit display".

COL: When COL = 1, the R61505 halts 32 grayscale amplifiers to display in 8-colors with low power consumption. When setting 8-color display mode, follow the sequence of 8-color display mode setting.

Table 12

COL	Operating Amplifier	Display Color
0	32	262,144
1	2	8

Note: When COL = 1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

GON, DTE: The combination of GON and DTE settings set the output level form gate lines (G1 ~ G320). When GON = 0, the Vcom output level becomes the GND level.

Table 13

APE	GON	DTE	G1~G320
0	*	*	VGL (= GND)
1	0	0	VGH
	0	1	VGH
	1	0	VGL
	1	1	VGH/VGL

VON: Controls VcomH, VcomL, Vcom amplitude signal output.

Table 14

APE	VON	VcomH/VcomL Output	Vcom Output
0	*	GND	GND
1	0	GND	GND
	1	Output VcomH, VcomL	Vcom amplitude: VcomH/VcomL

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The R61505 drives liquid crystal with non-lit display level or drives only partial image display areas.
BASEE = 1: A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

PTDE[1:0]: PTDE[0] is the display enable bit of partial image 1. PTDE[1] is the display enable bit of partial image 2. When PTDE1/0 = 0, the partial image is turned off and only base image is displayed on the screen. When PTDE1/0 = 1, the partial image is displayed on the screen. In this case, turn off the base image by setting BASEE = 0.

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP [3]	FP [2]	FP [1]	FP [0]	0	0	0	0	BP [3]	BP [2]	BP [1]	BP [0]
Default value		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP [3:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

BP [3:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Note on Setting BP and FP

Set the BP and FP bits as follows in respective operation modes.

Table 15 BP and FP Settings

Internal clock operation mode	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
RGB interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Table 16 Front and Back Porch Period (Line Periods)

FP[3:0] BP[3:0]	Front and Back Porch Period (Line Periods)
4'h0	Setting inhibited
4'h1	Setting inhibited
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
4'h5	5 lines
4'h6	6 lines
4'h7	7 lines
4'h8	8 lines
4'h9	9 lines
4'hA	10 lines
4'hB	11 lines
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting inhibited

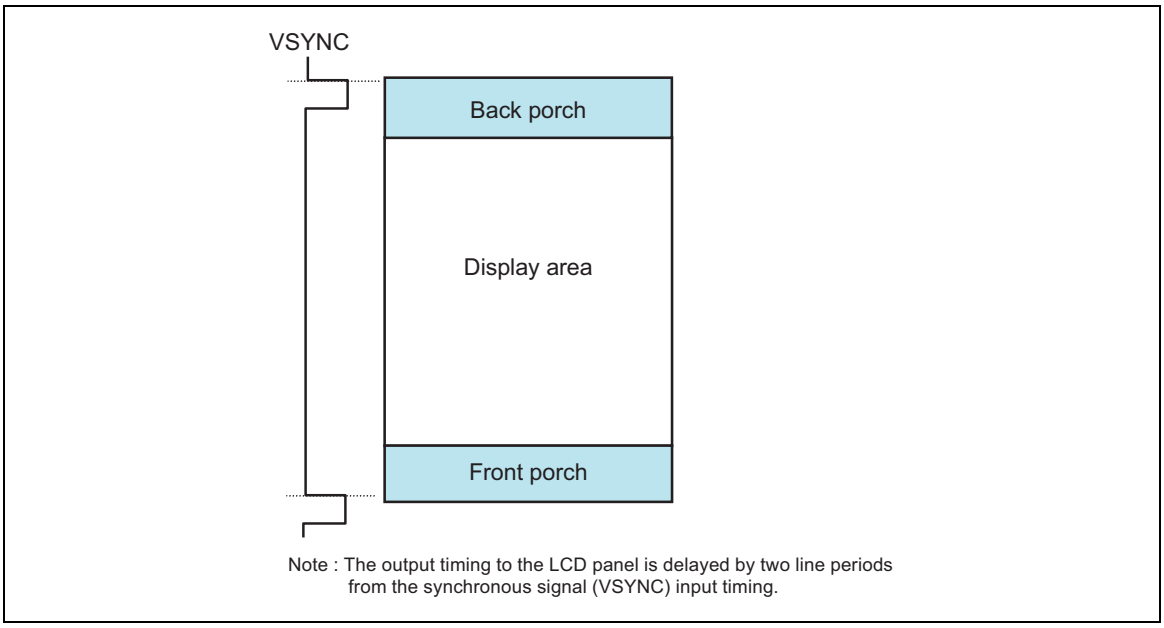


Figure 5 Front and Back Porch Periods

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS [2]	PTS [1]	PTS [0]	0	0	PTG [1]	PTG [0]	ICS [3]	ICS [2]	ICS [1]	ICS [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ICS[3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 17

ISC[3:0]	Scan Cycle	Time for Interval when (fFLM) = 60Hz
4'h1	Setting disabled	-
4'h2	3 frames	50ms
4'h3	5 frames	84ms
4'h4	7 frames	117ms
4'h5	9 frames	150ms
4'h6	11 frames	184ms
4'h7	13 frames	217ms
4'h8	15 frames	251ms

ISC[3:0]	Scan Cycle	Time for Interval when (fFLM) = 60Hz
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTG[1:0]: Sets the scan mode in non-display area. The scan mode selected by PTG[1:0] bits is applied in the non-display area when the base image is turned off and the non-display area other than the first and second partial display areas.

Table 18

PTG[1:0]	Scan Mode in Non-Display Area	Source Output Level in Non-Display Area	Vcom Output
2'h0	Normal scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h1	Setting disabled	-	-
2'h2	Interval scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h3	Setting disabled	-	-

Note: Select frame-inversion AC drive when interval scan is selected.

PTS[2:0]: Sets the source output level in non-display area drive period. When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V31 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 19 Source Output Level and Voltage Generating Operation in Non-Display Drive Period

PTS[2:0]	Source Output Level		Grayscale Amplifier in Operation	Step-Up Clock Frequency
	Positive Polarity	Negative Polarity		
3'h0	V31	V0	V0 to V31	Register setting (DC0, DC1)
3'h1	Setting inhibited	Setting inhibited	-	-
3'h2	GND	GND	V0 to V31	Register setting (DC0, DC1)
3'h3	Hi-Z	Hi-Z	V0 to V31	Register setting (DC0, DC1)
3'h4	V31	V0	V0 and V31	1/2 the frequency set by DC0, DC1
3'h5	Setting inhibited	Setting inhibited	-	-
3'h6	GND	GND	V0 and V31	1/2 the frequency set by DC0, DC1
3'h7	Hi-Z	Hi-Z	V0 and V31	1/2 the frequency set by DC0, DC1

Notes: 1. The power efficiency improved by halting grayscale amplifiers and slowing down the step-up clock frequency can be obtained in non-display drive period.

2. The gate output level in non-display drive period is controlled by the PTG setting (off-scan mode).

Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI [2]	FMI [1]	FMI [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE: When FMARKOE = 1, the R61505 starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits. See "FMARK " for details.

Table 20

FMI[2]	FMI[1]	FMI[0]	Output Interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	ENC [2]	ENC [1]	ENC [0]	0	0	0	RM	0	0	DM [1]	DM [0]	0	0	RIM [1]	RIM [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets the interface format when RGB interface is selected by RM and DM bits. Set RIM[1:0] bits before starting display operation via RGB interface. Do not change the setting while the R61505 performs display operation.

Table 21 RGB Interface Operation

RIM[1:0]	RGB Interface Operation	Colors
2'h0	18-bit RGB interface (1 transfer/pixel) via DB17-0	262,144
2'h1	16-bit RGB interface (1 transfer/pixel) via DB17-13 and DB11-1	65,536
2'h2	6-bit RGB interface (3 transfers/pixel) via DB17-12	262,144
2'h3	Setting inhibited	-

Notes: 1: Instruction bits are set via system interface.

2: Transfer the RGB dot data one by one in synchronization with DOTCLK in 6-bit RGB interface operation.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

Table 22 Display Interface

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting inhibited

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

Table 23 RAM Access Interface

RM	RAM Access Interface
0	System interface/VSYNC interface
1	RGB interface

ENC[2:0]: Sets the RAM write cycle via RGB interface.

Table 25 RAM Write Cycle

ENC[2:0]	RAM Write Cycle (Frame Periods)
3'h0	1 frame
3'h1	2 frames
3'h2	3 frames
3'h3	4 frames
3'h4	5 frames
3'h5	6 frames
3'h6	7 frames
3'h7	8 frames

Frame Marker Position (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	FMP [8]	FMP [7]	FMP [6]	FMP [5]	FMP [4]	FMP [3]	FMP [2]	FMP [1]	FMP [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is outputted at the start of back porch period for 1H period (IOVcc-IOGND amplitude signal). FMARK can be used as the trigger signal for frame synchronous write operation. See "FMARK " for details.

Make sure the setting restriction 9'h000 ≤ FMP ≤ BP+NL+FP.

Table 24

FMP[8:0]	FMARK Output Position
9''h000	0th line
9'h001	1st line
9''h002	2nd line
:	:
9''h175	373rd line
9'h176	374th line
9''h177	375th line

External Display Interface Control 2 (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of DOTCLK pin.

DPL = 0: input data on the rising edge of DOTCLK
DPL = 1: input data on the falling edge of DOTCLK

EPL: Sets the signal polarity of ENABLE pin.

EPL = 0: writes data DB17-0 when ENABLE = “0” and disables data write operation when ENABLE = “1”.
EPL = 1: writes data DB17-0 when ENABLE = “1” and disables data write operation when ENABLE = “0”.

HSPL: Sets the signal polarity of HSYNC pin.

HSPL = 0: low active
HSPL = 1: high active

VSPL: Sets the signal polarity of VSYNC pin.

VSPL = 0: low active
VSPL = 1: high active

Power Control

Power Control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	SAP	BT [3]	BT [2]	BT [1]	BT [0]	APE	0	AP [1]	AP [0]	0	DSTB	SLP	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AP[1:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP1-0 = 2'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

Table 25 Constant Current in Amplifier in LCD Power Supply, Grayscale Voltage Generating Circuits

AP[1:0]	LCD Power Supply Circuits	Grayscale Voltage Generating Circuit
2'h0	Halt operation	Halt operation
2'h1	0.5	0.62
2'h2	0.75	0.71
2'h3	1	1

Note: In this table, the constant current in operational amplifiers is the ratio to the constant current when AP[1:0] is set to 2'h3.

SAP: The grayscale voltage generating circuit is halted by setting SAP = 0. Grayscale voltages are generated when SAP = 1. When starting the operation of LCD power supply circuit in Power ON operation and so on, make sure SAP = 0. Set SAP = 1, after starting up the LCD power supply circuit.

BT[3:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

APE: Liquid crystal power supply enable bit. Set APE = 1 and follow the sequence when starting up the liquid crystal power supply.

Table 26

APE	Liquid Crystal Power Supply Circuit	Grayscale Voltage Generating Circuit
0	Halt	Halt
1	Operate	Operate

SLP: When SLP = 1, the R61505 enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change to the GRAM data and instruction setting is accepted and he GRAM data and the instruction setting are maintained in sleep mode.

DSTB: When DSTB = 1, the R61505 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the R61505 enters the deep standby mode, and they must be reset after exiting deep standby mode.

Table 27 Step-Up Factor and Output Voltage Level

BT[3:0]	DDVDH	VCL	VGH	VGL	Capacitor Connection Pins
4'h0	Vci1 x 2 [x 2]	-Vci1 [x –1]	DDVDH x 4 [x 8]	–(Vci1 + DDVDH x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'h1				–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
4'h2				–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'h3			Vci1 + DDVDH x 3 [x 7]	–(Vci1 + DDVDH x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'h4				–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
4'h5				–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'h6			DDVDH x 3 [x 6]	–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
4'h7				–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±
4'h8	Vci1 x 3 [x 3]		DDVDH x 4 [x 12]	–(Vci1 + DDVDH x 2) [x –7]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'h9				–(DDVDH x 2) [x –6]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
4'hA				–(Vci1 + DDVDH) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'hB			Vci1 + DDVDH x 3 [x 10]	–(Vci1 + DDVDH x 2) [x –7]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'hC				–(DDVDH x 2) [x –6]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
4'hD				–(Vci1 + DDVDH) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'hE			DDVDH x 3 [x 9]	–(DDVDH x 2) [x –6]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
4'hF				–(Vci1 + DDVDH) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±

Notes: 1. The step-up factor from Vci1 is shown in the brackets [ ].
2. Connect capacitors where required when using DDVDH, VGH, VGL, VCL voltages.
3. Set the following voltages within the respective ranges:
DDVDH = 6.0V (max.), VGH = 15.0V (max.), and VGL = –12.5V (max.), VCL = –3.0V (max).

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	DC1 [2]	DC1 [1]	DC1 [0]	0	DC0 [2]	DC0 [1]	DC0 [0]	0	VC [2]	VC [1]	VC [0]
Default value		0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0

Table 28 Step-Up Frequency (Step-Up Circuit 1)

DC0[2:0]	Step-Up Circuit 1: Step-Up Frequency (f_{DCDC1})
3'h0	fosc
3'h1	fosc / 2
3'h2	fosc / 4
3'h3	fosc / 8
3'h4	fosc / 16
3'h5	Setting inhibited
3'h6	Halt Step-up circuit 1
3'h7	Setting inhibited

Note: Make sure the DC0, DC1 setting restriction: $f_{DCDC1} \geq f_{DCDC2}$.

Table 29 Step-Up Frequency (Step-Up Circuit 2)

DC1[2:0]	Step-Up Circuit 2: Step-Up Frequency (f_{DCDC2})
3'h0	fosc / 16
3'h1	fosc / 32
3'h2	fosc / 64
3'h3	fosc / 128
3'h4	fosc / 256
3'h5	Setting inhibited
3'h6	Halt Step-up circuit 2
3'h7	Setting inhibited

Note: Make sure the DC0, DC1 setting restriction: $f_{DCDC1} \geq f_{DCDC2}$.

Table 30 VciOUT Output Level

VC[2:0]	VciOUT (Reference Voltage) (Vci1 Voltage)
3'h0	0.94 x VciLVL
3'h1	0.89 x VciLVL
3'h2	Setting inhibited
3'h3	Setting inhibited
3'h4	0.76 x VciLVL
3'h5	Setting inhibited
3'h6	Setting inhibited
3'h7	1.00 x VciLVL

Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VCMR[0]	0	0	PSON	PON	VRH [3]	VRH [2]	VRH [1]	VRH [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VRH[3:0]: Sets the factor to generate VREG1OUT from VciLVL.

Table 31 VREG1OUT

VRH[3:0]	VREG1OUT Voltage
4'h0 – 4'h3	Halt (Hi-Z)
4'h4 – 4'h7	Setting inhibited
4'h8	VciLVL x 1.60
4'h9	VciLVL x 1.65
4'hA	VciLVL x 1.70
4'hB	VciLVL x 1.75
4'hC	VciLVL x 1.80
4'hD	VciLVL x 1.85
4'hE	VciLVL x 1.90
4'hF	Setting inhibited

Note: Make sure the VC and VRH setting restrictions: VREG1OUT ≤ (DDVDH-0.5)V. When the load is on current to the maximum, VREG1OUT ≦ (DDVDH – 0.3V is also possible.

PON: Controls the operation to generate VLOUT3. In setting the PON bit, follows the power-supply startup sequence.

PON = 0: Halts the step-up operation to generate VLOUT3.
PON = 1: Starts the step-up operation to generate VLOUT3.

PSON: Power supply ON bit. When turning on the power supply, set PSE = 1 first and then set PSON = 1 to start internal power supply operation.

VCMR[0]: Selects either external resistance (VcomR pin) or internal electronic volume (VCM[4:0]) to set the electrical potential of VcomH. The internal electronic volume can be set by VCM bits

Table 32

VCMR[0]	VcomH Electrical Potential Setting
0	VcomR
1	Internal electronic volume

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	VDV [3]	VDV [2]	VDV [1]	VDV [0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[3:0]: Select the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.00.

Table 33

VDV[3:0]	Vcom Amplitude (VCS)	VDV[3:0]	Vcom Amplitude (VCS)
4'h0	VREG1OUT x 0.70	4'h8	VREG1OUT x 0.86
4'h1	VREG1OUT x 0.72	4'h9	VREG1OUT x 0.88
4'h2	VREG1OUT x 0.74	4'hA	VREG1OUT x 0.90
4'h3	VREG1OUT x 0.76	4'hB	VREG1OUT x 0.82
4'h4	VREG1OUT x 0.78	4'hC	VREG1OUT x 0.94
4'h5	VREG1OUT x 0.80	4'hD	VREG1OUT x 0.96
4'h6	VREG1OUT x 0.82	4'hE	VREG1OUT x 0.98
4'h7	VREG1OUT x 0.84	4'hF	VREG1OUT x 1.00

Note: Set VDV[3:0] so that Vcom amplitude becomes 6V or less.

Power Control 5 (R15h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	BLDM	0	0	0	0	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BLDM: Selects operation in normal mode and low power mode.

Table 34

BLDM	Vcom Operation
0	Normal operation
1	Low power mode

Note: Vcom low power mode depends on each panel characteristics. Confirm low power mode and image quality before using.

Power Control 6 (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PSE: Power supply startup enable bit. The R61505's power supply is started by setting PSON when PSE =1. When completing the power supply generating operation, PSE is set to 0.

RAM Access Instruction

RAM Address Set (Horizontal Address) (R20h)
RAM Address Set (Vertical Address) (R21h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R20	W	1	0	0	0	0	0	0	0	0	AD [7]	AD [6]	AD [5]	AD [4]	AD [3]	AD [2]	AD [1]	AD [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R21	W	1	0	0	0	0	0	0	0	AD [16]	AD [15]	AD [14]	AD [13]	AD [12]	AD [11]	AD [10]	AD [9]	AD [8]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the R61505 writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM = "1"), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

Note 2: In internal clock operation and VSYNC interface operation (RM = "0"), the address AD16-0 is set when executing the instruction.

Table 35 GRAM Address Setting Range

AD[16:0]	GRAM Data Setting
17'h00000 – 17'h000EF	Bitmap data on the first line
17'h00100 – 17'h001EF	Bitmap data on the second line
17'h00200 – 17'h002EF	Bitmap data on the third line
17'h00300 – 17'h003EF	Bitmap data on the fourth line
17'h00400 – 17'h004EF	Bitmap data on the fifth line
:	:
17'h16400 – 17'h13CEF	Bitmap data on the 317th line
17'h16500 – 17'h13DEF	Bitmap data on the 318th line
17'h16600 – 17'h13EEF	Bitmap data on the 319th line
17'h16700 – 17'h13FEF	Bitmap data on the 320th line

RAM Data Write (R22h)

R/W	RS	
W	1	RAM data write (WD[17:0]) bits are sent according to the selected format.
RGB interface		RAM data write (WD[17:0]) bits are sent according to the selected format.

WD[17:0]: The R61505 develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation.

The GRAM data represents the grayscale level. The R61505 automatically updates the address according to AM and I/D[1:0] settings as it writes data in the GRAM. The DFM bit sets the format to develop 16-bit data into the 18-bit data in 16-bit or 8-bit interface operation.

Note: When writing data in the GRAM via system interface while using the RGB interface, make sure that write operations via two interfaces do not conflict one another.

Table 36 GRAM Data and Corresponding LCD Grayscale Level (REV =1)

GRAM Data RGB	Grayscale Level	
	Negative	Positive
6'h00	V31	V0
6'h01	(V30+V31)/2	(V0+V1)/2
6'h02	V30	V1
6'h03	(V29+V30)/2	(V1+V2)/2
6'h04	V29	V2
6'h05	(V28+V29)/2	(V2+V3)/2
6'h06	V28	V3
6'h07	(V27+V28)/2	(V3+V4)/2
6'h08	V27	V4
6'h09	(V26+V27)/2	(V4+V5)/2
6'h0A	V26	V5
6'h0B	(V25+V26)/2	(V5+V6)/2
6'h0C	V25	V6
6'h0D	(V24+V25)/2	(V6+V7)/2
6'h0E	V24	V7
6'h0F	(V23+V24)/2	(V7+V8)/2
6'h10	V23	V8
6'h11	(V22+V23)/2	(V8+V9)/2
6'h12	V22	V9
6'h13	(V21+V22)/2	(V9+V10)/2
6'h14	V21	V10
6'h15	(V20+V21)/2	(V10+V11)/2
6'h16	V20	V11
6'h17	(V19+V20)/2	(V11+V12)/2
6'h18	V19	V12
6'h19	(V18+V19)/2	(V12+V13)/2
6'h1A	V18	V13
6'h1B	(V17+V18)/2	(V13+V14)/2
6'h1C	V17	V14
6'h1D	(V16+V17)/2	(V14+V15)/2
6'h1E	V16	V15
6'h1F	(V15+V16)/2	(V15+V16)/2

GRAM Data RGB	Grayscale Level	
	Negative	Positive
6'h20	V15	V16
6'h21	(V14+V15)/2	(V16+V17)/2
6'h22	V14	V17
6'h23	(V13+V14)/2	(V17+V18)/2
6'h24	V13	V18
6'h25	(12+V13)/2	(V18+V19)/2
6'h26	V12	V19
6'h27	(11V12)/2	(V19+V20)/2
6'h28	V11	V20
6'h29	(V10+V11)/2	(V20+V21)/2
6'h2A	V10	V21
6'h2B	(V9+V10)/2	(V21+V22)/2
6'h2C	V9	V22
6'h2D	(V8+V9)/2	(V22+V23)/2
6'h2E	V8	V23
6'h2F	(V7+V8)/2	(V23+V24)/2
6'h30	V7	V24
6'h31	(V6+V7)/2	(V24+V25)/2
6'h32	V6	V25
6'h33	(V5+V6)/2	(V25+V26)/2
6'h34	V5	V26
6'h35	(V4+V5)/2	(V26+V27)/2
6'h36	V4	V27
6'h37	(V3+V4)/2	(V27+V28)/2
6'h38	V3	V28
6'h39	(V2+V3)/2	(V28+V29)/2
6'h3A	V2	V29
6'h3B	(V1+V2)/2	(V29+V30)/2
6'h3C	V1	V30
6'h3D	(V0+V1)/2	(V30+V31)/2
6'h3E	(V1+2V0)/3	(V30+2V31)/3
6'h3F	V0	V31

Note: (Vn+Vn+1)/2, (Vn+2Vn+1)/3 are the effective grayscale levels by FRC (frame rate control).

Table 37 GRAM Data and Corresponding LCD Grayscale Level (REV =0)

GRAM Data RGB	Grayscale Level	
	Negative	Positive
6'h00	V0	V31
6'h01	(V0+V1)/2	(V30+V31)/2
6'h02	V1	V30
6'h03	(V1+V2)/2	(V29+V30)/2
6'h04	V2	V29
6'h05	(V2+V3)/2	(V28+V29)/2
6'h06	V3	V28
6'h07	(V3+V4)/2	(V27+V28)/2
6'h08	V4	V27
6'h09	(V4+V5)/2	(V26+V27)/2
6'h0A	V5	V26
6'h0B	(V5+V6)/2	(V25+V26)/2
6'h0C	V6	V25
6'h0D	(V6+V7)/2	(V24+V25)/2
6'h0E	V7	V24
6'h0F	(V7+V8)/2	(V23+V24)/2
6'h10	V8	V23
6'h11	(V8+V9)/2	(V22+V23)/2
6'h12	V9	V22
6'h13	(V9+V10)/2	(V21+V22)/2
6'h14	V10	V21
6'h15	(V10+V11)/2	(V20+V21)/2
6'h16	V11	V20
6'h17	(V11+V12)/2	(V19+V20)/2
6'h18	V12	V19
6'h19	(V12+V13)/2	(V18+V19)/2
6'h1A	V13	V18
6'h1B	(V13+V14)/2	(V17+V18)/2
6'h1C	V14	V17
6'h1D	(V14+V15)/2	(V16+V17)/2
6'h1E	V15	V16
6'h1F	(V15+V16)/2	(V15+V16)/2

GRAM Data RGB	Grayscale Level	
	Negative	Positive
6'h20	V16	V15
6'h21	(V16+V17)/2	(V14+V15)/2
6'h22	V17	V14
6'h23	(V17+V18)/2	(V13+V14)/2
6'h24	V18	V13
6'h25	(V18+V19)/2	(12+V13)/2
6'h26	V19	V12
6'h27	(V19+V20)/2	(11V12)/2
6'h28	V20	V11
6'h29	(V20+V21)/2	(V10+V11)/2
6'h2A	V21	V10
6'h2B	(V21+V22)/2	(V9+V10)/2
6'h2C	V22	V9
6'h2D	(V22+V23)/2	(V8+V9)/2
6'h2E	V23	V8
6'h2F	(V23+V24)/2	(V7+V8)/2
6'h30	V24	V7
6'h31	(V24+V25)/2	(V6+V7)/2
6'h32	V25	V6
6'h33	(V25+V26)/2	(V5+V6)/2
6'h34	V26	V5
6'h35	(V26+V27)/2	(V4+V5)/2
6'h36	V27	V4
6'h37	(V27+V28)/2	(V3+V4)/2
6'h38	V28	V3
6'h39	(V28+V29)/2	(V2+V3)/2
6'h3A	V29	V2
6'h3B	(V29+V30)/2	(V1+V2)/2
6'h3C	V30	V1
6'h3D	(V30+V31)/2	(V0+V1)/2
6'h3E	(V30+2V31)/3	(V1+2V0)/3
6'h3F	V31	V0

Note: (Vn+Vn+1)/2, (Vn+2Vn+1)/3 are the effective grayscale levels by FRC (frame rate control).

RAM Data Read (R22h)

R/W	RS	
R	1	RAM data read (RD[17:0]) bits are sent according to the selected interface format.

RD[17:0]: 18-bit data read from the GRAM. RAM data read RD[17:0] is transferred via different data bus in different interface operation.

When the R61505 reads data from the GRAM to the microcomputer, the first word read immediately after RAM address set is executed is taken in the internal read-data latch and invalid data is sent to the data bus. Valid data is sent to the data bus when the R61505 reads out the second and subsequent words.

When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.

Note: This register is not available in RGB interface operation.

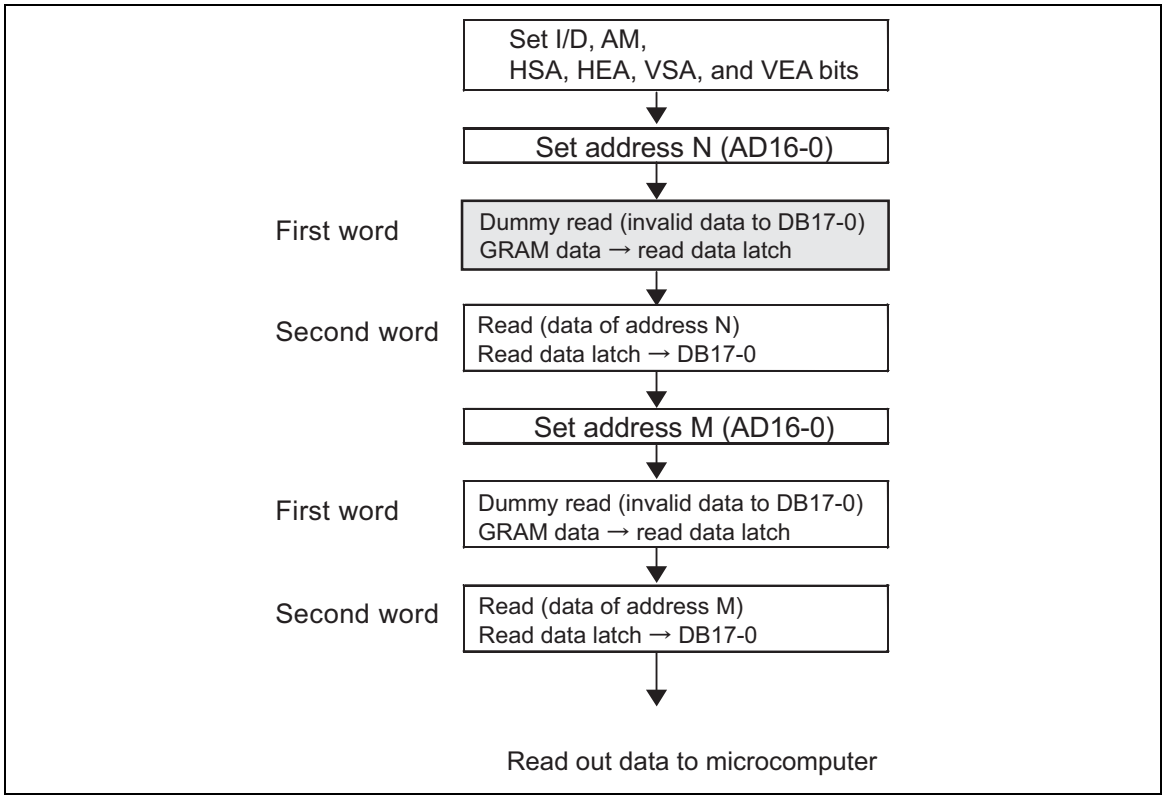


Figure 6 GRAM Read Sequence

VCOM Potential Setting

Power Control 7 (R29h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VCM 1[4]	VCM 1[3]	VCM 1[2]	VCM 1[1]	VCM 1[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM1[4:0]: Sets a factor of VREG1OUT from 0.69 to 1.00 to generate the VcomH voltage (Higher level of Vcom alternating voltage). VcomH voltage can be set either by internal electronic volume or external resistor. Set the VCMR bit to select either external resistor or internal electronic volume for VcomH adjustment.

Table 38

VCM1[4:0]	VCOMH Voltage	VCM1[4:0]	VCOMH Voltage
5'h00	VREG1OUT x 0.69	5'h10	VREG1OUT x 0.85
5'h01	VREG1OUT x 0.70	5'h11	VREG1OUT x 0.86
5'h02	VREG1OUT x 0.71	5'h12	VREG1OUT x 0.87
5'h03	VREG1OUT x 0.72	5'h13	VREG1OUT x 0.88
5'h04	VREG1OUT x 0.73	5'h14	VREG1OUT x 0.89
5'h05	VREG1OUT x 0.74	5'h15	VREG1OUT x 0.90
5'h06	VREG1OUT x 0.75	5'h16	VREG1OUT x 0.91
5'h07	VREG1OUT x 0.76	5'h17	VREG1OUT x 0.92
5'h08	VREG1OUT x 0.77	5'h18	VREG1OUT x 0.93
5'h09	VREG1OUT x 0.78	5'h19	VREG1OUT x 0.94
5'h0A	VREG1OUT x 0.79	5'h1A	VREG1OUT x 0.95
5'h0B	VREG1OUT x 0.80	5'h1B	VREG1OUT x 0.96
5'h0C	VREG1OUT x 0.81	5'h1C	VREG1OUT x 0.97
5'h0D	VREG1OUT x 0.82	5'h1D	VREG1OUT x 0.98
5'h0E	VREG1OUT x 0.83	5'h1E	VREG1OUT x 0.99
5'h0F	VREG1OUT x 0.84	5'h1F	VREG1OUT x 1.00

Notes: 1. Set the VcomH voltage between 3.0V to (DDVDH+0.5)V.

2. The VCM1[4:0] setting is enabled when selecting internal electronic volume adjustment by setting VCMR[0] = 1.

γ Control

γ Control 1 ~ 14 (R30h to R3Dh)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	P0KP1[2]	P0KP1[1]	P0KP1[0]	0	0	0	0	0	P0KP0[2]	P0KP0[1]	P0KP0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31	W	1	0	0	0	0	0	P0KP3[2]	P0KP3[1]	P0KP3[0]	0	0	0	0	0	P0KP2[2]	P0KP2[1]	P0KP2[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R32	W	1	0	0	0	0	0	P0KP5[2]	P0KP5[1]	P0KP5[0]	0	0	0	0	0	P0KP4[2]	P0KP4[1]	P0KP4[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R33	W	1	0	0	0	0	0	0	P0FP1[1]	P0FP1[0]	0	0	0	0	0	0	P0FP0[1]	P0FP0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R34	W	1	0	0	0	0	0	0	P0FP3[1]	P0FP3[0]	0	0	0	0	0	0	P0FP2[1]	P0FP2[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R35	W	1	0	0	0	0	0	P0RP1[2]	P0RP1[1]	P0RP1[0]	0	0	0	0	0	P0RP0[2]	P0RP0[1]	P0RP0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R36	W	1	0	0	0	V0RP1[4]	V0RP1[3]	V0RP1[2]	V0RP1[1]	V0RP1[0]	0	0	0	V0RP0[4]	V0RP0[3]	V0RP0[2]	V0RP0[1]	V0RP0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R37	W	1	0	0	0	0	0	P0KN1[2]	P0KN1[1]	P0KN1[0]	0	0	0	0	0	P0KN0[2]	P0KN0[1]	P0KN0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R38	W	1	0	0	0	0	0	P0KN3[2]	P0KN3[1]	P0KN3[0]	0	0	0	0	0	P0KN2[2]	P0KN2[1]	P0KN2[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R39	W	1	0	0	0	0	0	P0KN5[2]	P0KN5[1]	P0KN5[0]	0	0	0	0	0	P0KN4[2]	P0KN4[1]	P0KN4[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

γ Control 1 ~ 14 (R30h to R3Dh) (continued)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R 3A	W	1	0	0	0	0	0	0	P0FN 1[1]	P0FN 1[0]	0	0	0	0	0	0	P0FN 0[1]	P0FN 0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 3B	W	1	0	0	0	0	0	0	P0FN 3[1]	P0FN 3[0]	0	0	0	0	0	0	P0FN 2[1]	P0FN 2[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 3C	W	1	0	0	0	0	0	P0RN 1[2]	P0RN 1[1]	P0RN 1[0]	0	0	0	0	0	P0RN 0[2]	P0RN 0[1]	P0RN 0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 3D	W	1	0	0	0	V0R N1[4]	V0R N1[3]	V0R N1[2]	V0R N1[1]	V0R N1[0]	0	0	0	V0R N0[4]	V0R N0[3]	V0R N0[2]	V0R N0[1]	V0R N0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

P0KP5-0[2:0]: γ fine-adjustment register for positive polarity
P0FP3-0[1:0]: γ fine-adjustment register for positive polarity
P0RP1-0[2:0]: γ gradient-adjustment register for positive polarity
V0RP1-0[4:0]: γ amplitude-adjustment register for positive polarity
P0KN5-0[2:0]: γ fine-adjustment register for negative polarity
P0FN3-0[1:0]: γ fine-adjustment register for negative polarity
P0RN1-0[2:0]: γ gradient-adjustment register for negative polarity
V0RN1-0[4:0]: γ amplitude-adjustment register for negative polarity

Window Address Control Instruction

Window Horizontal RAM Address Start/End (R50h/ R51h)

Window Vertical RAM Address Start/End (R52h/R53h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R 50	W	1	0	0	0	0	0	0	0	0	HSA [7]	HSA [6]	HSA [5]	HSA [4]	HSA [3]	HSA [2]	HSA [1]	HSA [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 51	W	1	0	0	0	0	0	0	0	0	HEA [7]	HEA [6]	HEA [5]	HEA [4]	HEA [3]	HEA [2]	HEA [1]	HEA [0]
	Default value		0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R 52	W	1	0	0	0	0	0	0	0	VSA [8]	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 53	W	1	0	0	0	0	0	0	0	VEA [8]	VEA [7]	VEA [6]	VEA [5]	VEA [4]	VEA [3]	VEA [2]	VEA [1]	VEA [0]
	Default value		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HSA < HEA ≤ 8'hEF and 8'h04 ≤ HEA - HSA.

VSA[8:0], VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h13F.

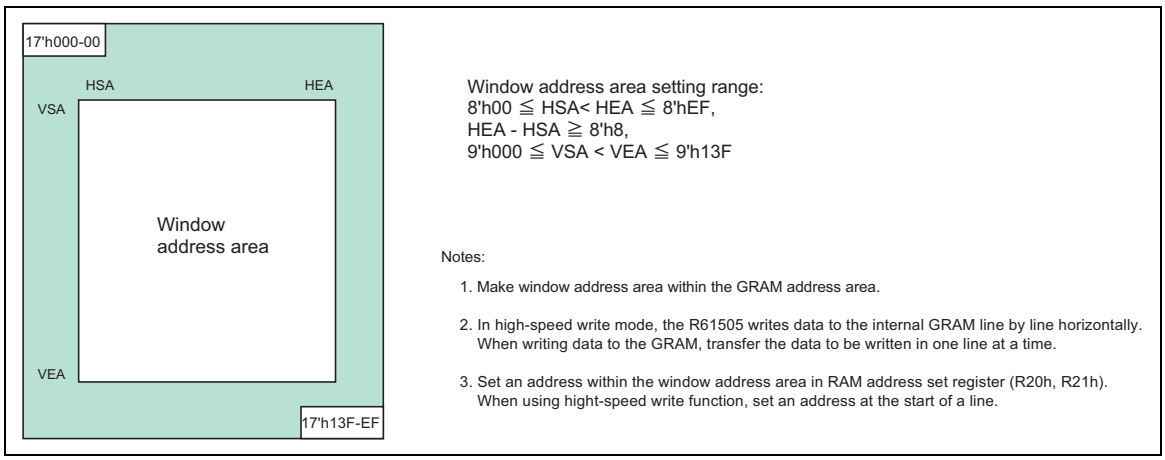


Figure 7 GRAM Address Map and Window Address Area

Base Image Display Control Instruction

Driver Output Control (R60h)

Base Image Display Control (R61h)

Vertical Scroll Control (R6Ah)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R60	W	1	GS	0	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	0	0	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R61	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6A	W	1	0	0	0	0	0	0	0	VL [8]	VL [7]	VL [6]	VL [5]	VL [4]	VL [3]	VL [2]	VL [1]	VL [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

GS: Sets the direction of scan by the gate driver. Set GS bit in combination with SM and SS bits for the convenience of the display module configuration and the display direction.

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the R61505 to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

Table 39 GRAM Data-Grayscale Level Inversion

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V31	V0
	:	:	:
	18'h3FFFFF	V0	V31
1	18'h00000	V0	V31
	:	:	:
	18'h3FFFFF	V31	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the R61505 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

Table 40

VLE	Base Image
0	Fixed
1	Enable scrolling

NDL: Sets the source output level in non-lit display area. NDL bit can keep the non-display area lit on.

Table 41

NDL	Non-Display Area	
	Positive	Negative
0	V31	V0
1	V0	V31

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0]. Make sure VL[8:0] ≤ 320.

Table 42

NL[5:0]	Number of Lines	NL[5:0]	Number of Lines	NL[5:0]	Number of Lines
6'h00	Setting inhibited	6'h0E	Setting inhibited	6'h1C	Setting inhibited
6'h01	Setting inhibited	6'h0F	Setting inhibited	6'h1D	240 (lines)
6'h02	Setting inhibited	6'h10	Setting inhibited	6'h1E	248
6'h03	Setting inhibited	6'h11	Setting inhibited	6'h1F	256
6'h04	Setting inhibited	6'h12	Setting inhibited	6'h20	264
6'h05	Setting inhibited	6'h13	Setting inhibited	6'h21	272
6'h06	Setting inhibited	6'h14	Setting inhibited	6'h22	280
6'h07	Setting inhibited	6'h15	Setting inhibited	6'h23	288
6'h08	Setting inhibited	6'h16	Setting inhibited	6'h24	296
6'h09	Setting inhibited	6'h17	Setting inhibited	6'h25	304
6'h0A	Setting inhibited	6'h18	Setting inhibited	6'h26	312
6'h0B	Setting inhibited	6'h19	Setting inhibited	6'h27	320
6'h0C	Setting inhibited	6'h1A	Setting inhibited	6'h28-6'h3F	Setting inhibited
6'h0D	Setting inhibited	6'h1B	Setting inhibited		

Table 43

SCN[5:0]	Gate Line No (Scan Start Position)			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G225	G96
6'h0F	G121	G200	G241	G80
6'h10	G129	G192	G257	G64
6'h11	G137	G184	G273	G48
6'h12	G145	G176	G289	G32
6'h13	G153	G168	G305	G16
6'h14	G161	G160	G2	G319
6'h15	G169	G152	G18	G303
6'h16	G177	G144	G34	G287
6'h17	G185	G136	G50	G271
6'h18	G193	G128	G66	G255
6'h19	G201	G120	G82	G239
6'h1A	G209	G112	G98	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28-6'h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

Partial Display Control Instruction

Partial Image 1: Display Position (R80h), RAM Address (Start/End Line Address) (R81h/R82h)

Partial Image 2: Display Position (R83h), RAM Address (Start/End Line Address) (R84h/R85h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R80	W	1	0	0	0	0	0	0	0	PTDP 0[8]	PTDP 0[7]	PTDP 0[6]	PTDP 0[5]	PTDP 0[4]	PTDP 0[3]	PTDP 0[2]	PTDP 0[1]	PTDP 0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R81	W	1	0	0	0	0	0	0	0	PTSA 0[8]	PTSA 0[7]	PTSA 0[6]	PTSA 0[5]	PTSA 0[4]	PTSA 0[3]	PTSA 0[2]	PTSA 0[1]	PTSA 0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R82	W	1	0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R83	W	1	0	0	0	0	0	0	0	PTDP 1[8]	PTDP 1[7]	PTDP 1[6]	PTDP 1[5]	PTDP 1[4]	PTDP 1[3]	PTDP 1[2]	PTDP 1[1]	PTDP 1[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R84	W	1	0	0	0	0	0	0	0	PTSA 1[8]	PTSA 1[7]	PTSA 1[6]	PTSA 1[5]	PTSA 1[4]	PTSA 1[3]	PTSA 1[2]	PTSA 1[1]	PTSA 1[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R85	W	1	0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[8:0]: Sets the display position of partial image 1.
PTDP1[8:0]: Sets the display position of partial image 2.
The display areas of the partial images 1 and 2 must not overlap each another. In setting, make sure that

Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display position: (PTDP0, PTDP0 + (PTEA0 – PTSA0))
Coordinates of partial image 2 display position: (PTDP1, PTDP1 + (PTEA1 – PTSA1))

If PTDP0 = "9'h000", the partial image 1 is displayed from the first line of the base image.

PTSA0[8:0] and PTEA0[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 1. In setting, make sure that PTSA0 ≤ PTEA0.

PTSA1[8:0] and PTEA1[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 2. In setting, make sure that PTSA1 ≤ PTEA1.

Panel Interface Control Instruction

Panel Interface Control 1(R90h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI [1]	DIVI [0]	0	0	0	RTNI [4]	RTNI [3]	RTNI [2]	RTNI [1]	RTNI [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the R61505's display operation is synchronized with internal clock.

DIVI[1:0]: Sets the division ratio of the internal clock frequency. The R61505's internal operation is synchronized with the frequency divided internal clock. When DIVI[1:0] setting is changed, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see "Frame-Frequency Adjustment Function". The setting in DIVI[1:0] is disabled in RGB interface operation.

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{fosc}{\text{Clocks per line x division ratio x (line + BP + FP)}} \quad [Hz]$$

fosc : RC oscillation frequency
Line: Number of lines to drive the LCD (NL bits)
Division ratio: DIVI
Clocks per line: RTNI

Table 44 Clocks per Line (Internal Clock Operation: 1 Clock = 1 OSC)

RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line
5'h00-5'h0F	Setting inhibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

Table 45 Division ratio of the internal clock

DIVI[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

Panel Interface Control 2(R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation synchronizing with the internal clock.

Table 46

NOWI[2:0]	Non-Overlap Period	NOWI[2:0]	Non-Overlap Period
3'h0	0 (internal clock *see note)	3'h4	4 (internal clock *see note)
3'h1	1	3'h5	5
3'h2	2	3'h6	6
3'h3	3	3'h7	7

Note: The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits.

Panel Interface Control 3(R93h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI[2]	MCPI[1]	MCPI[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MCPI[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled in display operation synchronizing with the internal clock.

Table 47

MCPI[2:0]	Source Output Position	MCPI[2:0]	Source Output Position
3'h0	Setting disabled	3'h4	4
3'h1	1 (internal clock *see note)	3'h5	5
3'h2	2	3'h6	6
3'h3	3	3'h7	7

Note: The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits. The source output position is measured from the reference point by the number of internal clock cycle.

Panel Interface Control 4(R95h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE [1]	DIVE [0]	0	0	RTN E[5]	RTN E[4]	RTN E[3]	RTN E[2]	RTN E[1]	RTN E[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

RTNE[5:0]: Sets RTNE[5:0] and DIVE[1:0] bits so that the number of DOTCLK calculated from the following formula becomes the number of DOTCLK which should be inputted in 1H period. The RTNE[5:0] setting is enabled in display operation via RGB interface.

DIVE[1:0] (division ratio) x RTNE[5:0] (Number of DOTCLK) ≤ Number of DOTCLK in 1H period

DIVE[1:0]: Sets the division ratio of DOTCLK frequency. The R61505's internal operation is synchronized with the frequency divided DOTCLK. The setting in DIVE[1:0] is enabled in RGB interface operation.

Table 48 Division Ratio of DOTCLK

DIVE[1:0]	Division Ratio	Internal Operation Clock Unit (DOTCLK)			
		18-bit, 1 Transfer RGB interface	DOTCLK = 5 MHz	8-bit, 3 Transfers RGB Interface	DOTCLK = 15 MHz
2'h0	Setting disabled	Setting disabled	-	Setting disabled	-
2'h1	1/4	4 DOTCLKs	0.8μs	12 DOTCLKs	0.8μs
2'h2	1/8	8 DOTCLKs	1.6μs	24 DOTCLKs	1.6μs
2'h3	1/16	16 DOTCLKs	3.2μs	48 DOTCLKs	3.2μs

Table 49 DOTCLK per Line (1H period)

RTNE[5:0]	DOTCLK per Line (1H)	RTNE[5:0]	DOTCLK per Line (1H)
6'h00	Setting disabled	6'h20	32 clocks
6'h01	Setting disabled	6'h21	33 clocks
6'h02	Setting disabled	6'h22	34 clocks
6'h03	Setting disabled	6'h23	35 clocks
6'h04	Setting disabled	6'h24	36 clocks
6'h05	Setting disabled	6'h25	37 clocks
6'h06	Setting disabled	6'h26	38 clocks
6'h07	Setting disabled	6'h27	39 clocks
6'h08	Setting disabled	6'h28	40 clocks
6'h09	Setting disabled	6'h29	41 clocks
6'h0A	Setting disabled	6'h2A	42 clocks
6'h0B	Setting disabled	6'h2B	43 clocks
6'h0C	Setting disabled	6'h2C	44 clocks
6'h0D	Setting disabled	6'h2D	45 clocks
6'h0E	Setting disabled	6'h2E	46 clocks
6'h0F	Setting disabled	6'h2F	47 clocks
6'h10	16 clocks	6'h30	48 clocks
6'h11	17 clocks	6'h31	49 clocks
6'h12	18 clocks	6'h32	50 clocks
6'h13	19 clocks	6'h33	51 clocks
6'h14	20 clocks	6'h34	52 clocks
6'h15	21 clocks	6'h35	53 clocks
6'h16	22 clocks	6'h36	54 clocks
6'h17	23 clocks	6'h37	55 clocks
6'h18	24 clocks	6'h38	56 clocks
6'h19	25 clocks	6'h39	57 clocks
6'h1A	26 clocks	6'h3A	58 clocks
6'h1B	27 clocks	6'h3B	59 clocks
6'h1C	28 clocks	6'h3C	60 clocks
6'h1D	29 clocks	6'h3D	61 clocks
6'h1E	30 clocks	6'h3E	62 clocks
6'h1F	31 clocks	6'h3F	63 clocks

Panel Interface Control 5(R97h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	NOWE[3]	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOWE[3:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

Table 50

NOWE[3:0]	Non-Overlap Period	NOWE[3:0]	Non-Overlap Period
4'h0	0 (clock *see note)	4'h8	8 (clock *see note)
4'h1	1	4'h9	9
4'h2	2	4'hA	10
4'h3	3	4'hB	11
4'h4	4	4'hC	12
4'h5	5	4'hD	13
4'h6	6	4'hE	14
4'h7	7	4'hF	15

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) [DOTCLK].

Panel Interface Control 6(R98h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE[2]	MCPE[1]	MCPE[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MCPE[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled in display operation via RGB interface.

Table 51

MCPE[2:0]	Source Output Position	MCPE[2:0]	Source Output Position
3'h0	0 (clock *see note)	3'h4	4 (clock *see note)
3'h1	1	3'h5	5
3'h2	2	3'h6	6
3'h3	3	3'h7	7

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) [DOTCLK].

Oscillation Control Instruction

Oscillation Control (RA4h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALB: Prevents external clock frequency variance.

R61505 Instruction List

Rev1.2 '05/12/02

Main category			Sub category	Upper code								Lower code								Note
Upper index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
-	Index	—	Index	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID21	ID0	
0*	Display control	00h	Device code read	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1	Device code "1505"
		01h	Driver output control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0	
		02h	Liquid crystal drive waveform	0	0	0	0	0	1	BC0 (0)	EOR (0)	0	0	0	0	0	0	0	0	
		03h	Entry mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	I/D[1](1)	I/D[0](1)	AM (0)	0	0	0	
		04h	Resize control	0	0	0	0	0	0	RCV[1] (0)	RCV[0] (0)	0	0	RCH[1] (0)	RCH[0] (0)	0	0	RSZ[1] (0)	RSZ[0] (0)	
		05h-06h	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		07h	Display control 1	0	0	PTDE[1] (0)	PTDE[0] (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	COL (0)	0	D[1](0)	D[0](0)	
		08h	Display control 2	0	0	0	0	FP[3] (1)	FP[2] (0)	FP[1] (0)	FP[0] (0)	0	0	0	0	BP[3] (1)	BP[2] (0)	BP[1] (0)	BP[0] (0)	
		09h	Display control 3	0	0	0	0	0	PTS[2] (0)	PTS[1] (0)	PTS[0] (0)	0	0	PTG[1] (0)	PTG[0] (0)	ISC[3] (0)	ISC[2] (0)	ISC[1] (0)	ISC[0] (0)	
		0Ah	Display control 4	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE (0)	FMI[2] (0)	FMI[1] (0)	FMI[0] (0)	
		0Bh	Setting disabled	Setting disabled	setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		0Ch	External display interface control 1	0	ENC[2] (0)	ENC[1] (0)	ENC[0] (0)	0	0	0	RM (0)	0	0	DM[1] (0)	DM[0] (0)	0	0	RIM[1] (0)	RIM[0] (0)	
		0Dh	Frame marker control	0	0	0	0	0	0	0	FMP[8](0)	FMP[7](0)	FMP[6](0)	FMP[5](0)	FMP[4](0)	FMP[3](0)	FMP[2](0)	FMP[1](0)	FMP[0](0)	
		0Eh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		0Fh	External display interface control 2	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)	
1*	Power control	10h	Power control 1	0	0	0	SAP (0)	BT[3] (0)	BT[2] (0)	BT[1] (0)	BT[0] (0)	APE(0)	0	AP[1] (0)	AP[0] (0)	0	DSTB (0)	SLP (0)	0	
		11h	Power control 2	0	0	0	0	0	DC1[2] (1)	DC1[1] (1)	DC1[0] (0)	0	DC0[2] (1)	DC0[1] (1)	DC0[0] (0)	0	VC[2] (0)	VC[1] (0)	VC[0] (0)	
		12h	Power control 3	0	0	0	0	0	0	0	VCMR[0] (0)	0	0	PSON (0)	PON (0)	VRH[3] (0)	VRH[2] (0)	VRH[1] (0)	VRH[0] (0)	
		13h	Power control 4	0	0	0	0	VDV[3] (0)	VDV[2] (0)	VDV[1] (0)	VDV[0] (0)	0	0	0	0	0	0	0	0	
		14h	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		15h	Power control 5	0	0	0	BLDM (0)	0	0	1	1	0	1	0	1	0	0	0	0	
		16h	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		17h	Power control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE (0)	
		18h-1Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
2*	RAM access	20h	RAM address set (horizontal)	0	0	0	0	0	0	0	0	AD[7] (0)	AD[6] (0)	AD[5] (0)	AD[4] (0)	AD[3] (0)	AD[2] (0)	AD[1] (0)	AD[0] (0)	
	Power control	21h	RAM address set (vertical)	0	0	0	0	0	0	0	AD[16] (0)	AD[15] (0)	AD[14] (0)	AD[13] (0)	AD[12] (0)	AD[11] (0)	AD[10] (0)	AD[9] (0)	AD[8] (0)	
		22h	RAM data write/RAM data read	RAM data write (WD17-0)/RAM data read (RD17-0) bits are sent according to the selected interface format																
		23h-28h	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		29h	Power control 7	0	0	0	0	0	0	0	0	0	0	0	VCM1[4](0)	VCM1[3](0)	VCM1[2](0)	VCM1[1](0)	VCM1[0](0)	
		2Ah—2Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
3*	Gamma control	30h	Gamma control 1	0	0	0	0	0	P0KP1[2] (0)	P0KP1[1] (0)	P0KP1[0] (0)	0	0	0	0	0	P0KP0[2] (0)	P0KP0[1] (0)	P0KP0[0] (0)	
		31h	Gamma control 2	0	0	0	0	0	P0KP3[2] (0)	P0KP3[1] (0)	P0KP3[0] (0)	0	0	0	0	0	P0KP2[2] (0)	P0KP2[1] (0)	P0KP2[0] (0)	
		32h	Gamma control 3	0	0	0	0	0	P0KP5[2] (0)	P0KP5[1] (0)	P0KP5[0] (0)	0	0	0	0	0	P0KP4[2] (0)	P0KP4[1] (0)	P0KP4[0] (0)	
		33h	Gamma control 4	0	0	0	0	0	0	P0FP1[1] (0)	P0FP1[0] (0)	0	0	0	0	0	0	P0FP0[1] (0)	P0FP0[0] (0)	
		34h	Gamma control 5	0	0	0	0	0	0	P0FP3[1] (0)	P0FP3[0] (0)	0	0	0	0	0	0	P0FP2[1] (0)	P0FP2[0] (0)	
		35h	Gamma control 6	0	0	0	0	0	P0RP1[2] (0)	P0RP1[1] (0)	P0RP1[0] (0)	0	0	0	0	0	P0RP0[2] (0)	P0RP0[1] (0)	P0RP0[0] (0)	
		36h	Gamma control 7	0	0	0	V0RP1[4] (0)	V0RP1[3] (0)	V0RP1[2] (0)	V0RP1[1] (0)	V0RP1[0] (0)	0	0	0	V0RP0[4] (0)	V0RP0[3] (0)	V0RP0[2] (0)	V0RP0[1] (0)	V0RP0[0] (0)	
		37h	Gamma control 8	0	0	0	0	0	P0KN1[2] (0)	P0KN1[1] (0)	P0KN1[0] (0)	0	0	0	0	0	P0KN0[2] (0)	P0KN0[1] (0)	P0KN0[0] (0)	
		38h	Gamma control 9	0	0	0	0	0	P0KN3[2] (0)	P0KN3[1] (0)	P0KN3[0] (0)	0	0	0	0	0	P0KN2[2] (0)	P0KN2[1] (0)	P0KN2[0] (0)	
		39h	Gamma control 10	0	0	0	0	0	P0KN5[2] (0)	P0KN5[1] (0)	P0KN5[0] (0)	0	0	0	0	0	P0KN4[2] (0)	P0KN4[1] (0)	P0KN4[0] (0)	
		3Ah	Gamma control 11	0	0	0	0	0	0	P0FN1[1] (0)	P0FN1[0] (0)	0	0	0	0	0	0	P0FN0[1] (0)	P0FN0[0] (0)	
		3Bh	Gamma control 12	0	0	0	0	0	0	P0FN3[1] (0)	P0FN3[0] (0)	0	0	0	0	0	0	P0FN2[1] (0)	P0FN2[0] (0)	
		3Ch	Gamma control 13	0	0	0	0	0	P0RN1[2] (0)	P0RN1[1] (0)	P0RN1[0] (0)	0	0	0	0	0	P0RN0[2] (0)	P0RN0[1] (0)	P0RN0[0] (0)	
		3Dh	Gamma control 14	0	0	0	V0RN1[4] (0)	V0RN1[3] (0)	V0RN1[2] (0)	V0RN1[1] (0)	V0RN1[0] (0)	0	0	0	V0RN0[4] (0)	V0RN0[3] (0)	V0RN0[2] (0)	V0RN0[1] (0)	V0RN0[0] (0)	
		3Eh-3Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
4*	Setting disabled	40h-4Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
5*	Coordinate control	50h	Window horizontal RAM address (start)	0	0	0	0	0	0	0	0	HSA[7] (0)	HSA[6] (0)	HSA[5] (0)	HSA[4] (0)	HSA[3] (0)	HSA[2] (0)	HSA[1] (0)	HSA[0] (0)	
		51h	Window horizontal RAM address (end)	0	0	0	0	0	0	0	0	HEA[7] (1)	HEA[6] (1)	HEA[5] (1)	HEA[4] (0)	HEA[3] (1)	HEA[2] (1)	HEA[1] (1)	HEA[0] (1)	
		52h	Window vertical RAM address (start)	0	0	0	0	0	0	0	VSA[8] (0)	VSA[7] (0)	VSA[6] (0)	VSA[5] (0)	VSA[4] (0)	VSA[3] (0)	VSA[2] (0)	VSA[1] (0)	VSA[0] (0)	
		53h	Window vertical RAM address (end)	0	0	0	0	0	0	0	VEA[8] (1)	VEA[7] (0)	VEA[6] (0)	VEA[5] (1)	VEA[4] (1)	VEA[3] (1)	VEA[2] (1)	VEA[1] (1)	VEA[0] (1)	
		54h-5Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
6*	Screen display control	60h	Driver output control	GS (0)	0	NL[5] (0)	NL[4] (0)	NL[3] (0)	NL[2] (0)	NL[1] (0)	NL[0] (0)	0	0	SCN[5] (0)	SCN[4] (0)	SCN[3] (0)	SCN[2] (0)	SCN[1] (0)	SCN[0] (0)	
		61h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)	
		62h-69h	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		6Ah	Vertical scroll control	0	0	0	0	0	0	0	VL[8] (0)	VL[7] (0)	VL[6] (0)	VL[5] (0)	VL[4] (0)	VL[3] (0)	VL[2] (0)	VL[1] (0)	VL[0] (0)	
		6Bh-6Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
7*	Setting disabled	70h-7Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
8*	Partial control	80h	Partial image 1 display position	0	0	0	0	0	0	0	PTDP0[8] (0)	PTDP0[7] (0)	PTDP0[6] (0)	PTDP0[5] (0)	PTDP0[4] (0)	PTDP0[3] (0)	PTDP0[2] (0)	PTDP0[1] (0)	PTDP0[0] (0)	
		81h	Partial image 1 RAM area (start line)	0	0	0	0	0	0	0	PTSA0[8] (0)	PTSA0[7] (0)	PTSA0[6] (0)	PTSA0[5] (0)	PTSA0[4] (0)	PTSA0[3] (0)	PTSA0[2] (0)	PTSA0[1] (0)	PTSA0[0] (0)	
		82h	Partial image 1 RAM area (end line)	0	0	0	0	0	0	0	PTEA0[8] (0)	PTEA0[7] (0)	PTEA0[6] (0)	PTEA0[5] (0)	PTEA0[4] (0)	PTEA0[3] (0)	PTEA0[2] (0)	PTEA0[1] (0)	PTEA0[0] (0)	
		83h	Partial image 2 display position	0	0	0	0	0	0	0	PTDP1[8] (0)	PTDP1[7] (0)	PTDP1[6] (0)	PTDP1[5] (0)	PTDP1[4] (0)	PTDP1[3] (0)	PTDP1[2] (0)	PTDP1[1] (0)	PTDP1[0] (0)	
		84h	Partial image 2 RAM area (start line)	0	0	0	0	0	0	0	PTSA1[8] (0)	PTSA1[7] (0)	PTSA1[6] (0)	PTSA1[5] (0)	PTSA1[4] (0)	PTSA1[3] (0)	PTSA1[2] (0)	PTSA1[1] (0)	PTSA1[0] (0)	
		85h	Partial image 2 RAM area (end line)	0	0	0	0	0	0	0	PTEA1[8] (0)	PTEA1[7] (0)	PTEA1[6] (0)	PTEA1[5] (0)	PTEA1[4] (0)	PTEA1[3] (0)	PTEA1[2] (0)	PTEA1[1] (0)	PTEA1[0] (0)	
		86h-8Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
9*	Panel interface control	90h	Panel interface control 1	0	0	0	0	0	0	DIVI[1](0)	DIVI[0](0)	0	0	0	RTNI[4](1)	RTNI[3](0)	RTNI[2](0)	RTNI[1](0)	RTNI[0](0)	
		91h	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		92h	Panel interface control 2	0	0	0	0	0	NOWI[2](0)	NOWI[1](0)	NOWI[0](0)	0	0	0	0	0	0	0	0	
		93h	Panel interface control 3	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI[2](0)	MCPI[1](0)	MCPI[0](0)	
		94h	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		95h	Panel interface control 4	0	0	0	0	0	0	DIVE[1](1)	DIVE[0](0)	0	0	RTNE[5](0)	RTNE[4](1)	RTNE[3](1)	RTNE[2](1)	RTNE[1](1)	RTNE[0](0)	
		96h	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		97h	Panel interface control 5	0	0	0	0	NOWE[3](0)	NOWE[2](0)	NOWE[1](0)	NOWE[0](0)	0	0	0	0	0	0	0	0	
		98h	Panel interface control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE[2](0)	MCPE[1](0)	MCPE[0](0)	
		99h-9Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
A*	Oscillation control	A0h-A3h	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
		A4h	Oscillation control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB(0)	
		A5h-AFh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	
B*-F*	Setting disabled	F0h—F Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	Setting disabled	

Reset Function

The R61505 is initialized by the RESET input. During reset period, the R61505 is in a busy state and instruction from the MPU and GRAM access are not accepted. The R61505's internal power supply circuit unit is initialized also by the RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, GRAM access and initial instruction setting are prohibited.

1. Initial state of Instruction Bits (Default)

See the instruction list of p.79. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data Initialization

The RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period (D1-0 = "00").

3. Output Pin Initial State * see Note

1. LCD driver S1~S720 : GND
   G1~G320 : VGL (= GND)
2. Vcom : Halt (GND output)
3. VcomH : Vci
4. VcomL : Halt (GND output)
5. VREG1OUT : VGS
6. VciOUT : Hi-z
7. VLOUT1 : Vci
8. VLOUT2 : DDVDH (= Vci)
9. VLOUT3 : GND
10. VCL : GND
11. FMARK : Halt (GND output)
12. Oscillator : Oscillate
13. SDO : High level (IOVcc) when IM = "010*"(serial interface)
    : Hi-z when IM ≠ "010*"(other than serial interface)

4. Initial State of Input/Output Pins* see Note

1. C11+ : Hi-z
2. C11- : Hi-z
3. C12+ : Hi-z
4. C12- : Hi-z
5. C13+ : Vci1 (= Hi-z)
6. C13- : GND
7. C21+ : DDVDH (= Vci)
8. C21- : GND
9. C22+ : DDVDH (= Vci)
10. C22- : GND
11. C23+ : DDVDH (= Vci)
12. C23- : GND
13. VDD : VDD

Note: The above mentioned initial states of output and input pins are those of when the R61505's power supply circuit is connected as exemplified in "Connection Example".

5. Note on Reset Function

(1) When a RESET input is entered into the R61505 while it is in deep standby mode, the R61505 starts up the inside logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable. For this reason, do not enter a RESET input in deep standby mode.

(2) When transferring instruction in either two or three transfers via 8-/9-/16-bit interface, make sure to execute data transfer synchronization after reset operation.

Basic Mode Operation of the R61505

The basic operation modes of the R61505 are shown in the following diagram. When making a transition from one mode to another, refer to instruction setting sequence.

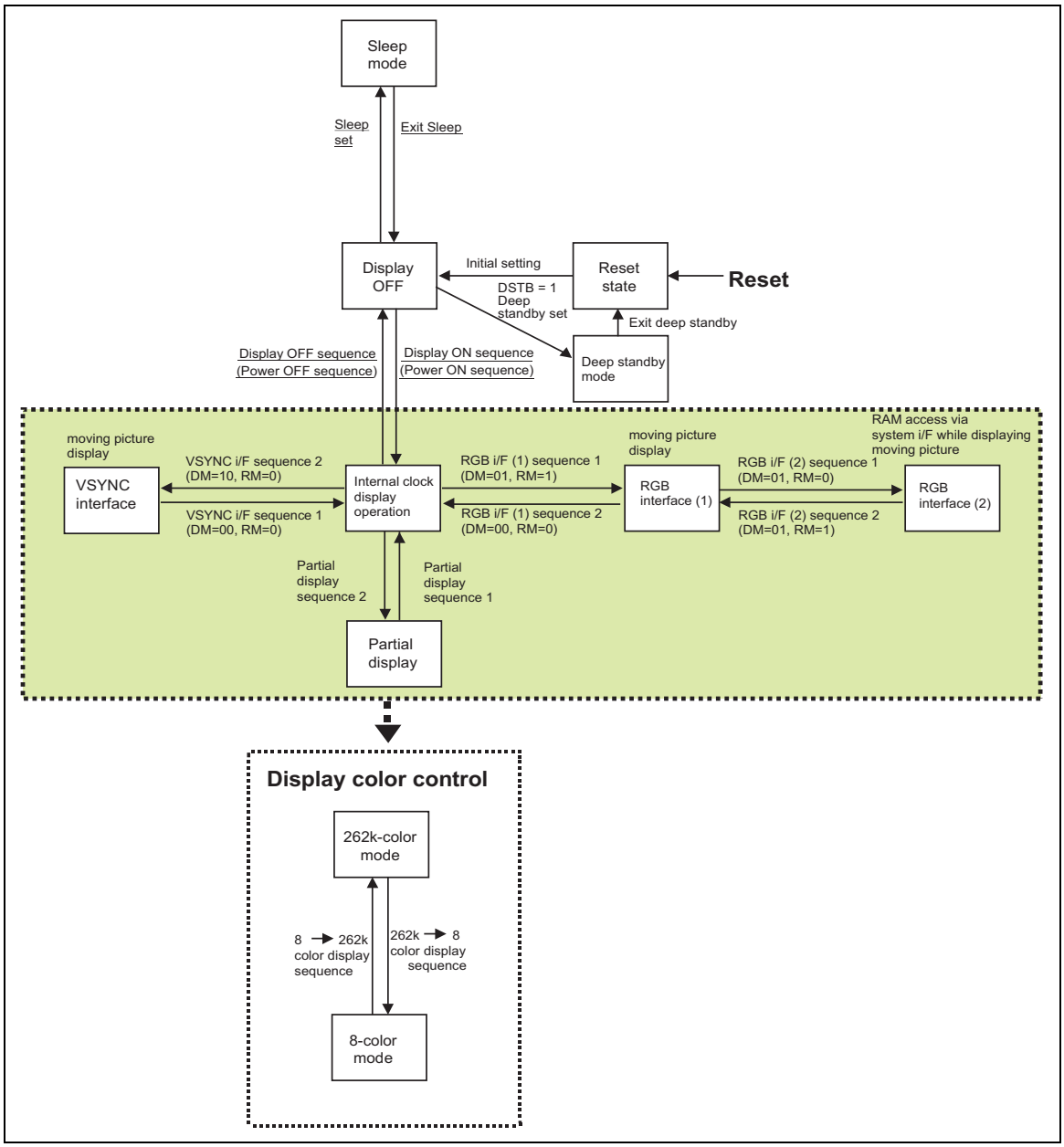


Figure 8

Interface and Data Format

The R61505 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The R61505 can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the R61505 supports RGB interface and VSYNC interface, which enables data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the R61505 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the R61505's GRAM so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the RAM area to write data for moving picture display, which enables displaying a moving picture and RAM data in other than the moving picture area simultaneously. To access the R61505's internal RAM in high speed with low power consumption, use high-speed write function (HWM = 1) in RGB or VSYNC interface operation.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The R61505 operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register (R0Ch). When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Table 52 Operation Modes

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes: 1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM1-0) while RGB interface is in operation.
4. See the "External Display Interface" section for the sequences when switching from one mode to another.
5. Use high-speed write function (HWM = 1) when writing data via RGB or VSYNC interface.

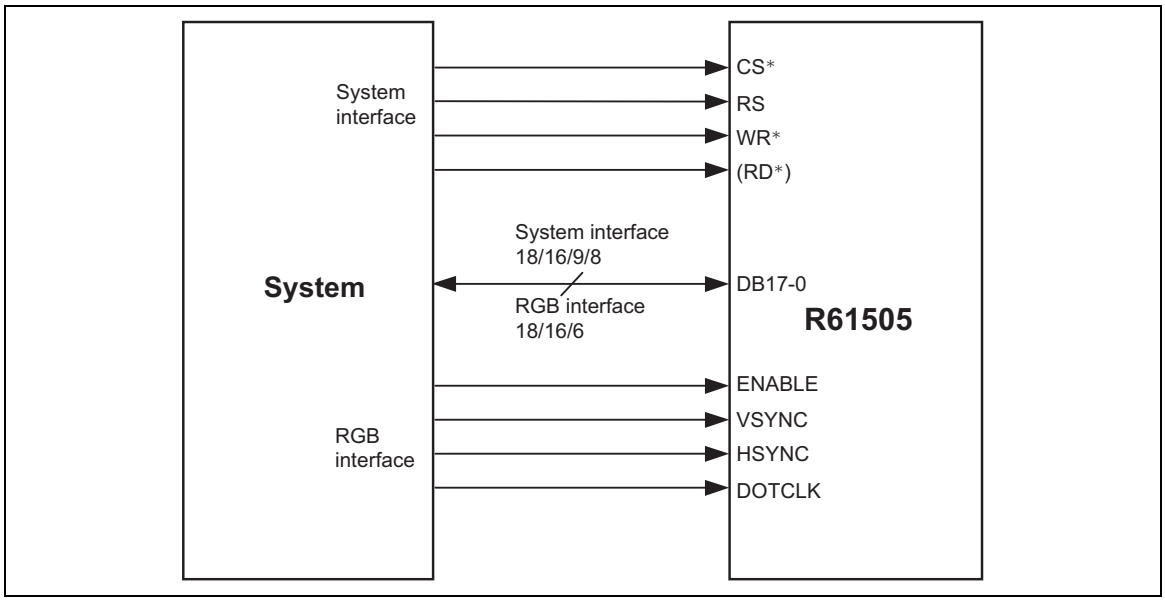


Figure 9

Internal Clock Operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

RGB Interface Operation (1)

The display operation is synchronized with frame synchronous signal (VSYNC), line synchronous signal (HSYNC), and dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied during the display operation via RGB interface.

The R61505 transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function can minimize the total number of data transfer for moving picture display by transferring only the data to be written in the moving picture RAM area when it is written and enables the R61505 to display a moving picture and the data in other than the moving picture RAM area simultaneously.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the R61505 by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with the setting of these periods.

RGB Interface Operation (2)

This mode enables the R61505 to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first. Then set an address in the RAM address set register and R22h in the index register.

VSYNC Interface Operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the R61505 to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the "VSYNC Interface" section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the R61505 according to the instruction settings for these periods.

System Interface

The following are the kinds of system interfaces available with the R61505. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 53 IM Bit Settings and System Interface

IM3	IM2	IM1	IM0	Interfacing Mode with MPU	DB Pins	Colors
0	0	0	0	Setting inhibited	-	-
0	0	0	1	Setting inhibited	-	-
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144 *see Note1
0	0	1	1	80-system 8-bit interface	DB17-10	262,144 *see Note2
0	1	0	*	Clock synchronous serial interface	-	65,536
0	1	1	0	Setting inhibited	-	-
0	1	1	1	Setting inhibited	-	-
1	0	0	0	Setting inhibited	-	-
1	0	0	1	Setting inhibited	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	262,144
1	0	1	1	80-system 9-bit interface	DB17-9	262,144
1	1	0	0	Setting inhibited	-	-
1	1	0	1	Setting inhibited	-	-
1	1	1	0	Setting inhibited	-	-
1	1	1	1	Setting inhibited	-	-

Notes: 1. 65,536 colors in 16-bit single transfer mode.
2. 65,536 colors in 8-bit 2-transfer mode.

80-System 18-Bit Bus Interface

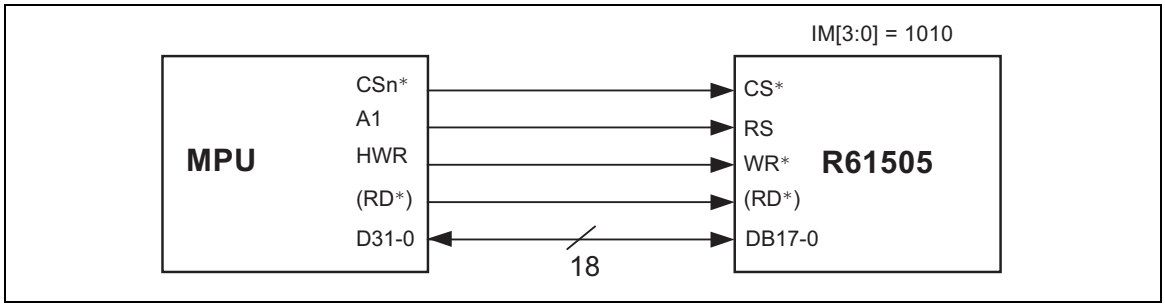


Figure 10 18-Bit Interface

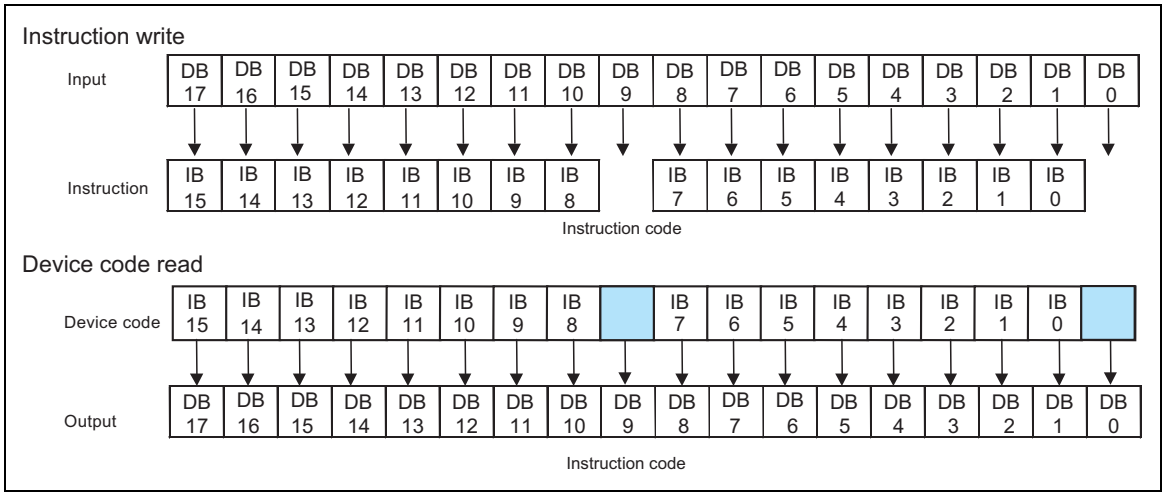


Figure 11 18-Bit Interface Data Format (Instruction Write / Device Code Read)

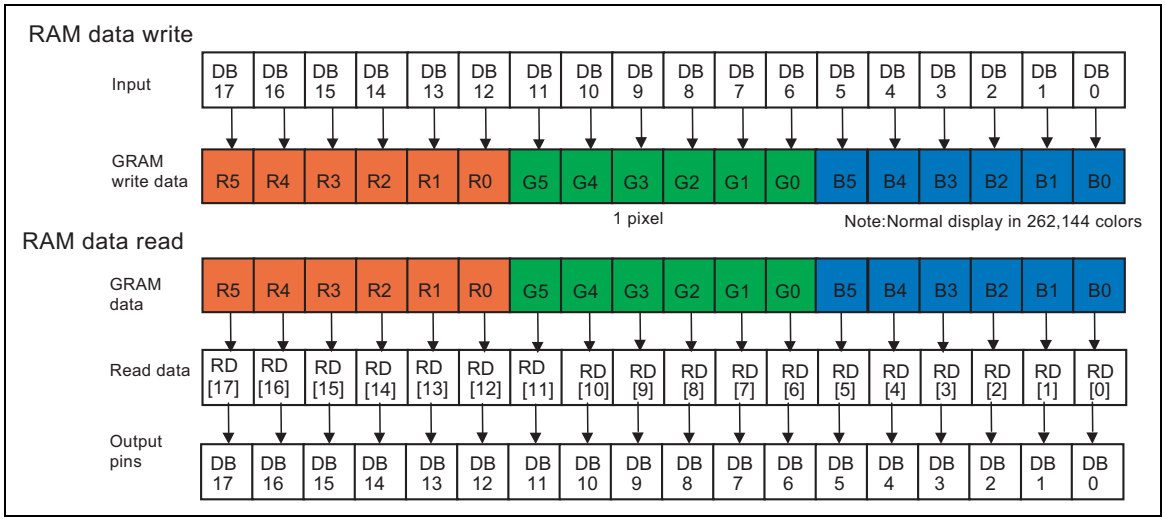


Figure 12 18-Bit Interface Data Format (RAM Data Write / RAM Data Read)

80-System 16-Bit Bus Interface

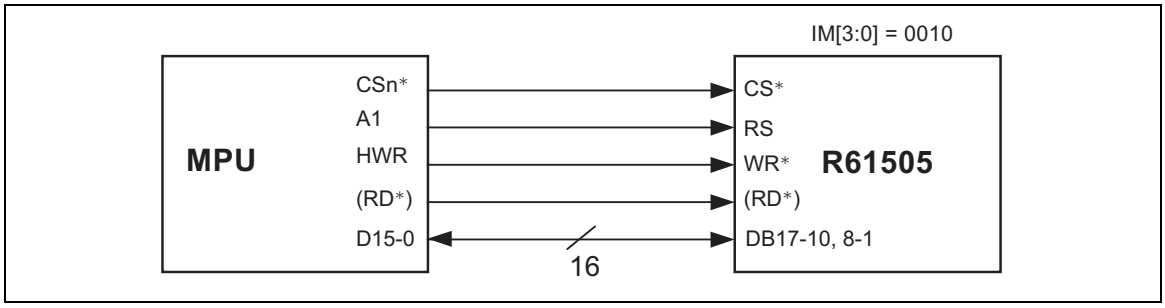


Figure 13 16-Bit Interface

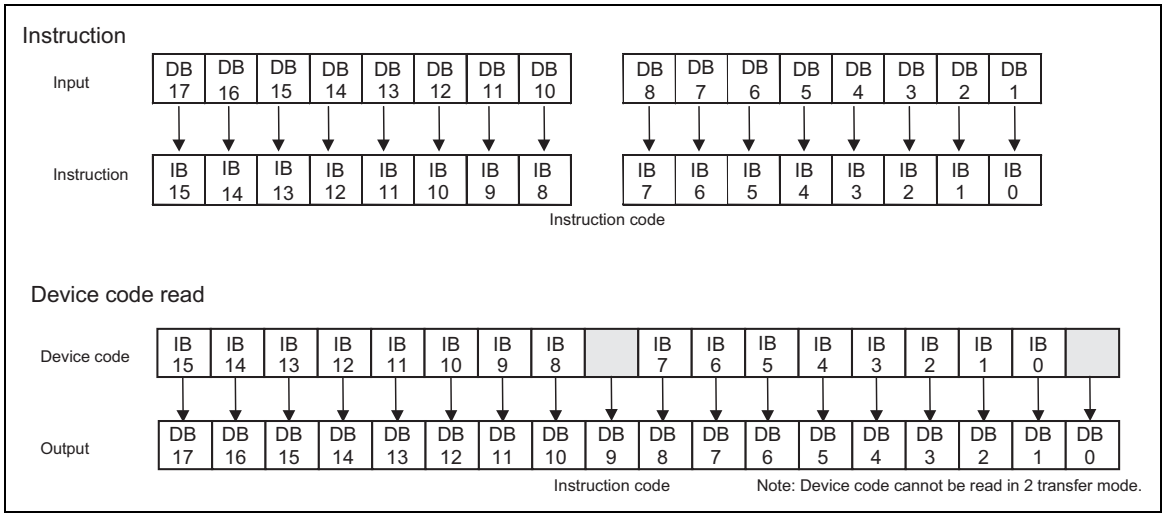


Figure 14 16-Bit Interface Data Format (Instruction Write / Device Code Read)

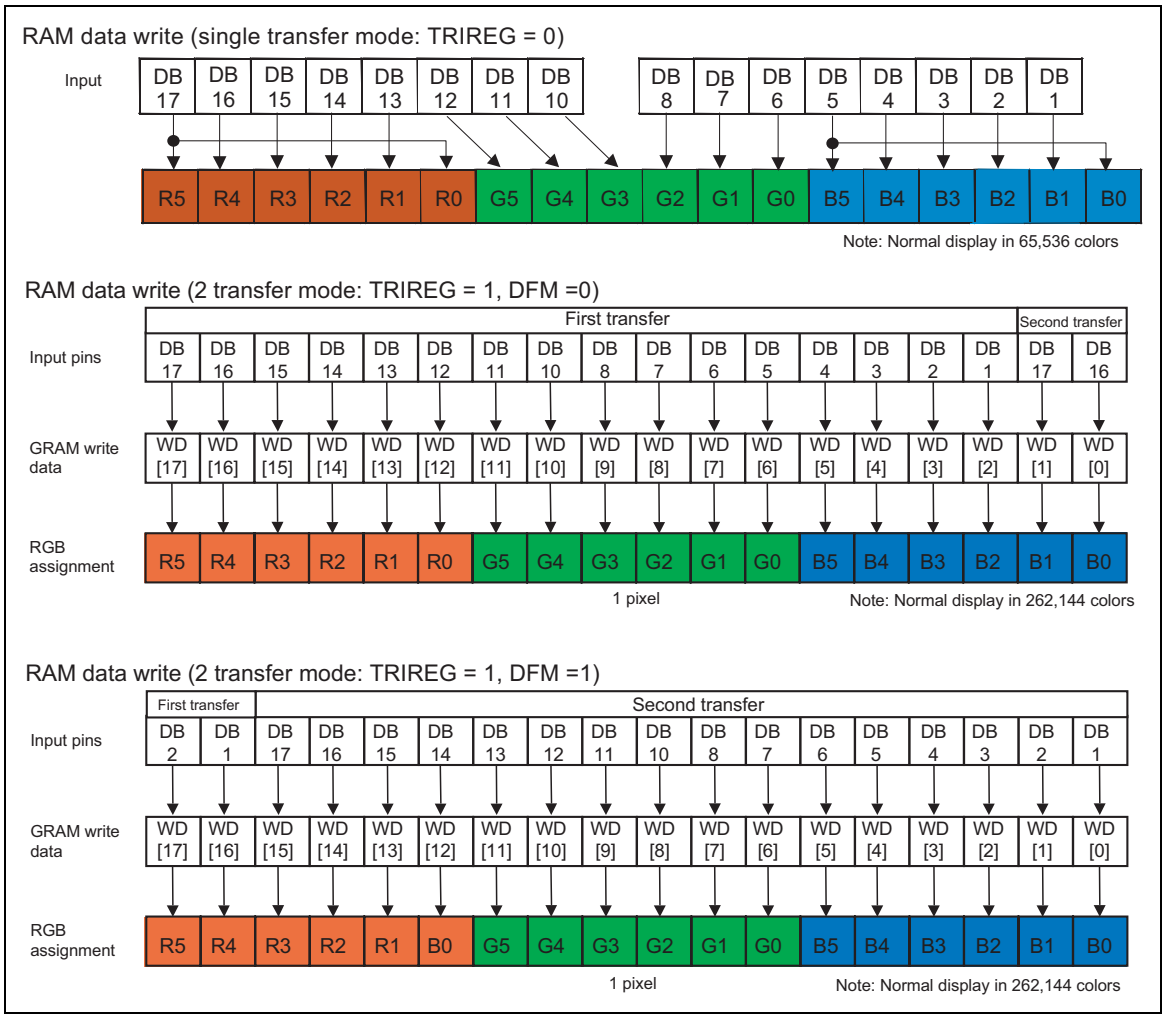


Figure 15 16-Bit Interface Data Format (RAM Data Write)

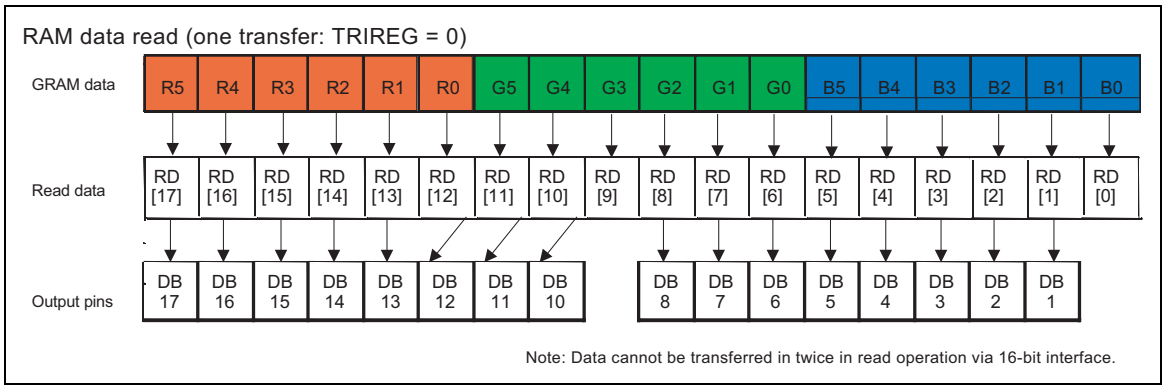


Figure 16 16-bit Interface Data Format (RAM Data Read)

Data Transfer Synchronization in 16-Bit Bus Interface Operation

The R61505 supports data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 2/16 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

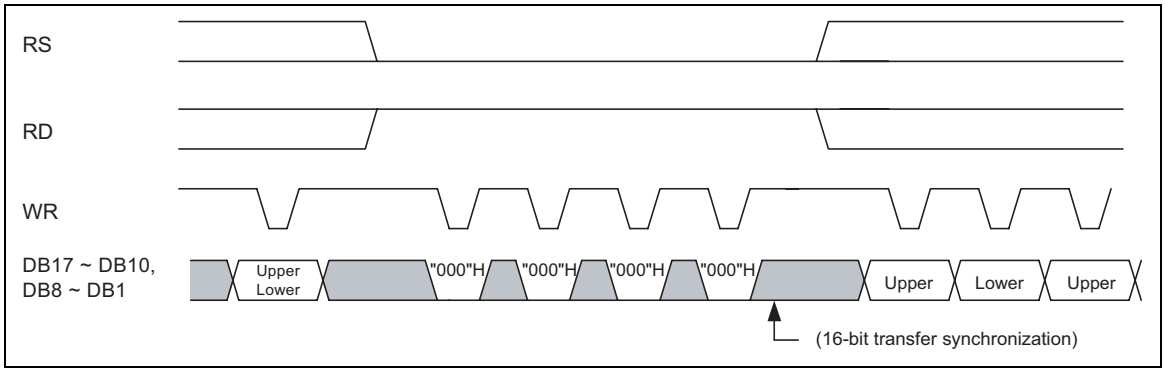


Figure 17 16-Bit Data Transfer Synchronization

80-System 9-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either IOVcc or IOGND level. When transferring the index register setting, make sure to write upper byte (8 bits).

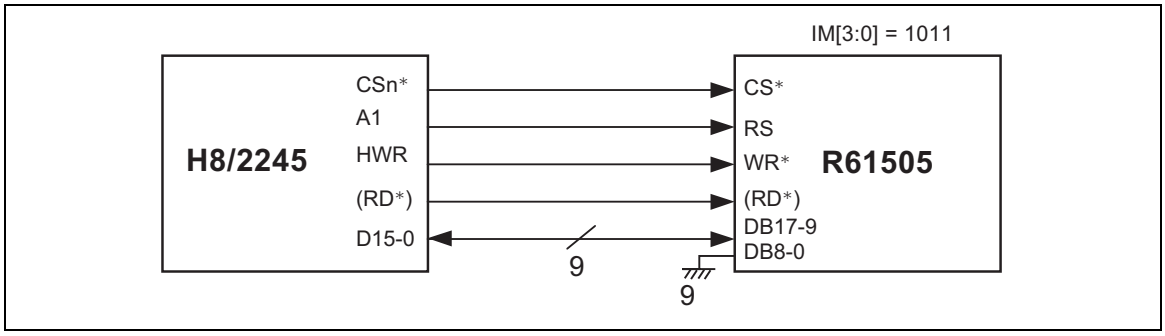


Figure 18 9-Bit interface

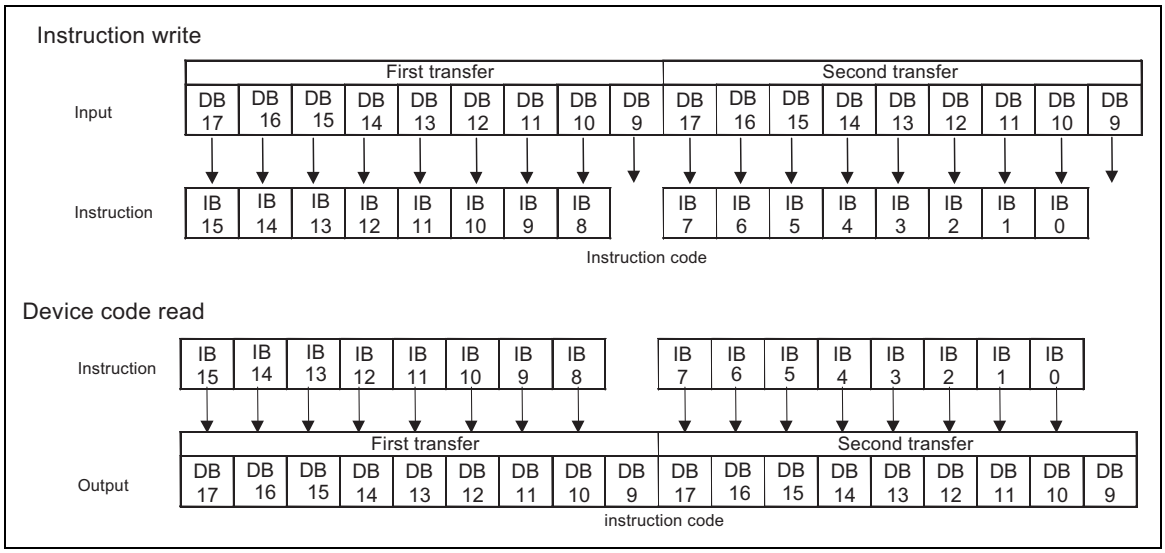


Figure 19 9-Bit Interface Data Format (Instruction Write / Device Code Read)

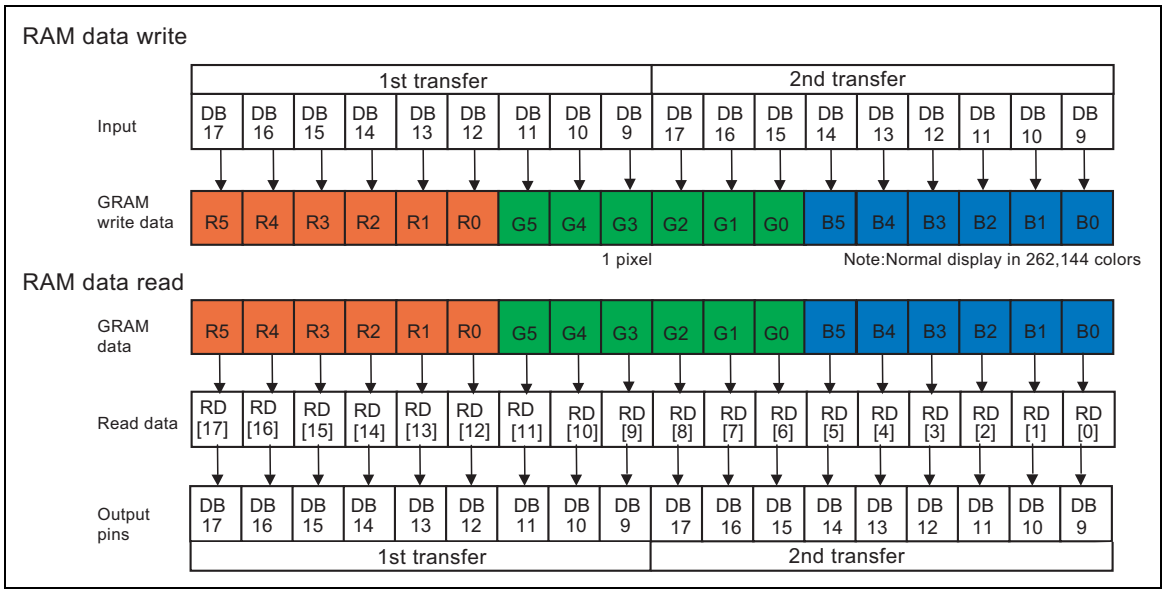


Figure 20 9-Bit Interface Data Format (RAM Data Write/ RAM Data Read)

Data Transfer Synchronization in 9-Bit Bus Interface Operation

The R61505 supports data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 9 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

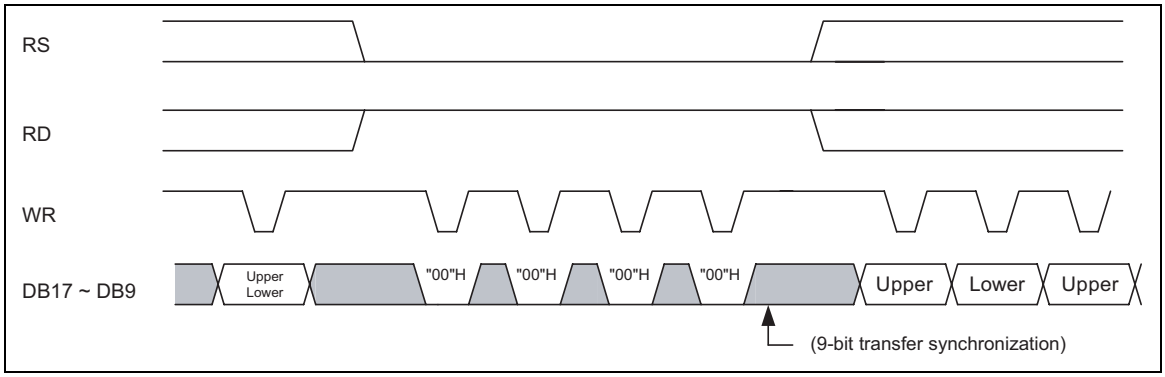


Figure 21 9-Bit Data Transfer Synchronization

80-System 8-Bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either IOVcc or IOGND level. When transferring the index register setting, make sure to write upper byte (8 bits).

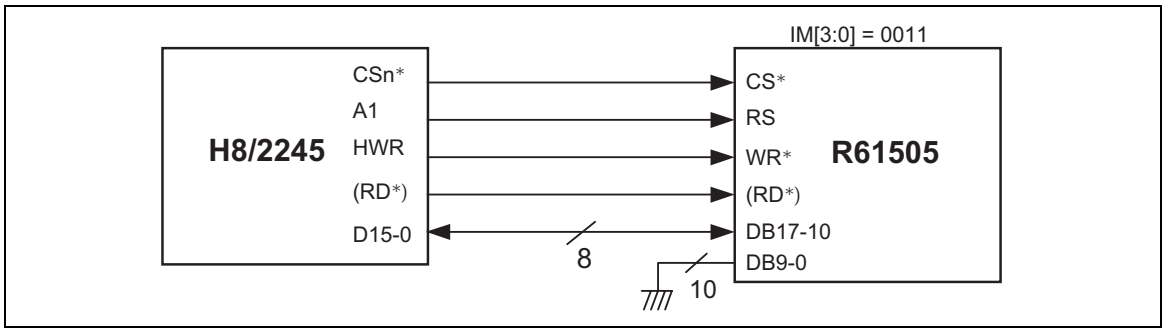


Figure 22 8-Bit Interface

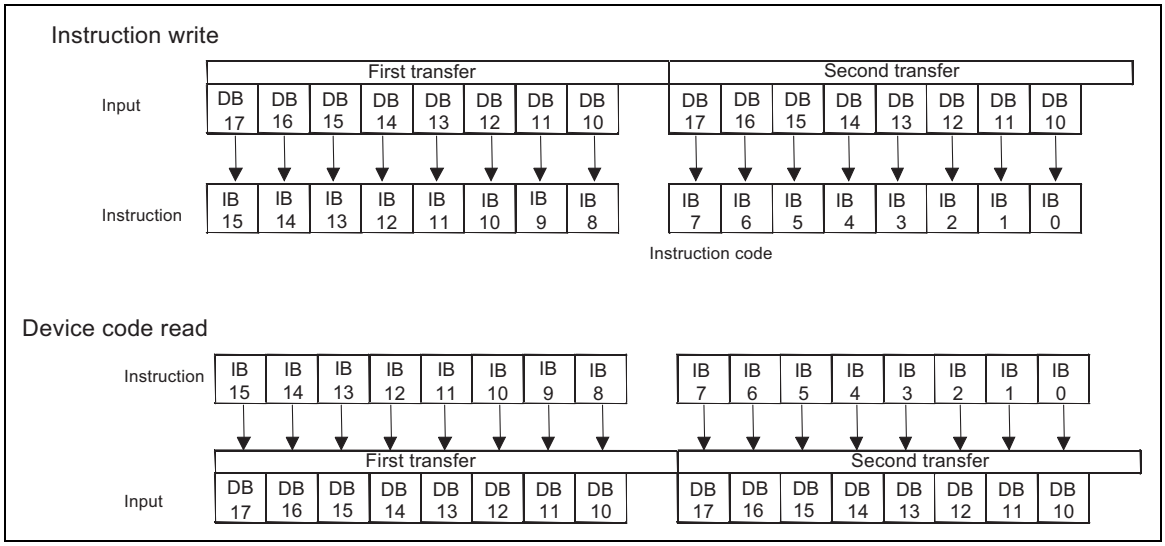


Figure 23 8-Bit Interface Data Format (Instruction Write / Device Code Read)

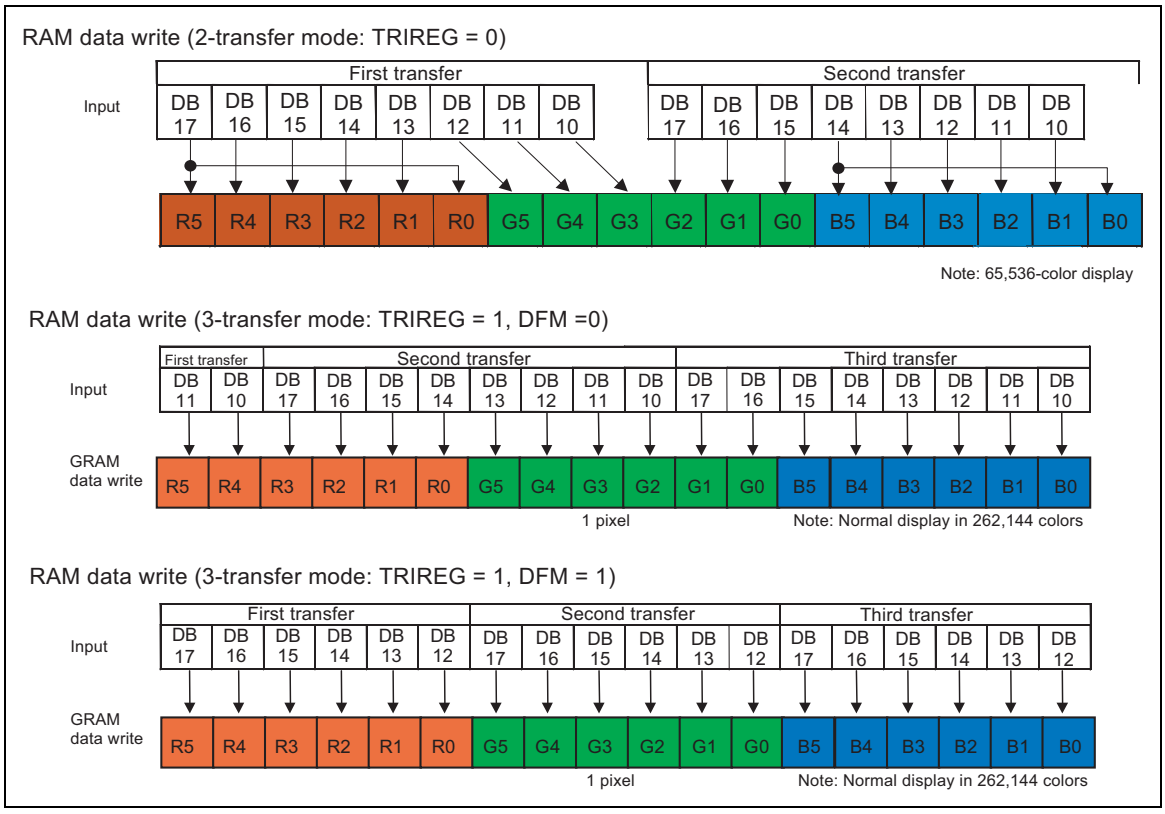


Figure 24 8-Bit Interface Data Format (RAM Data Write)

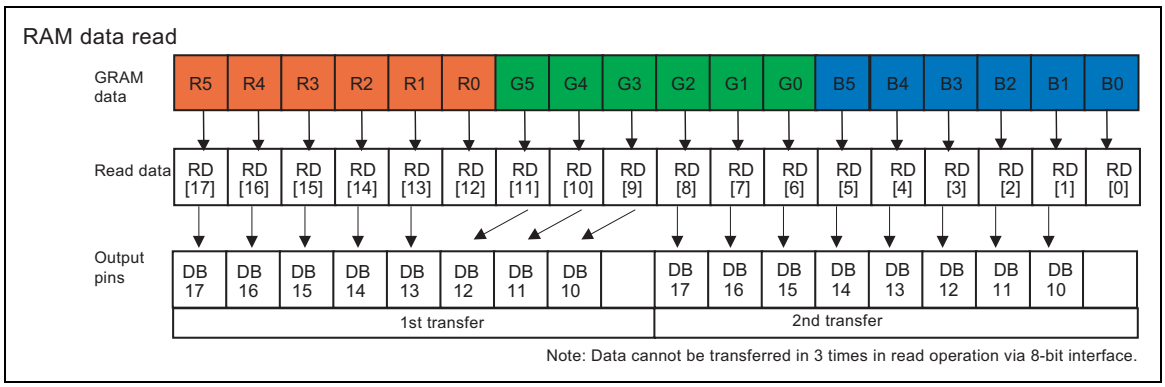


Figure 25 8-Bit Interface Data Format (RAM Data Read)

Data Transfer Synchronization in 8-Bit Bus Interface Operation

The R61505 supports data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 8 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

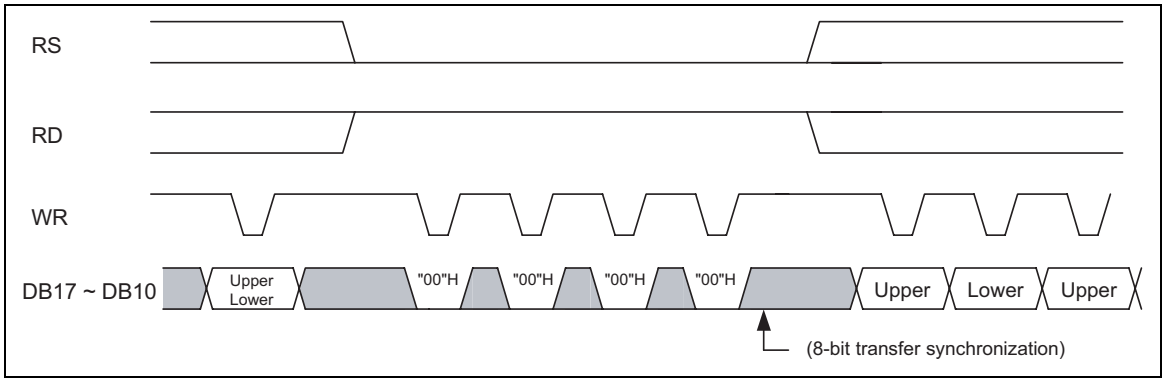


Figure 26 8-Bit Data Transfer Synchronization

Serial Interface

The serial interface is selected by setting the IM3/2/1 pins to the IOGND/IOVcc/IOGND levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVcc or GND level.

The R61505 recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The R61505 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the R61505 are compared and both 6-bit data match. Then, the R61505 starts taking in subsequent data. The least significant bit of the device identification code is determined by setting the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the R61505 because the seventh bit of the start byte is register select bit (RS). When RS = 0, index register write operation is executed. When RS = 1, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The R61505 receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The R61505 writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the R61505 starts transferring or receiving data in units of bytes. The R61505 transfers data from the MSB. The R61505's instruction consists of 16 bits and it is executed inside the R61505 after it is transferred in two bytes (16 bits: DB15-0) from the MSB. The R61505 expands RAM write data into 18 bits when writing them to the internal GRAM. The first byte received by the R61505 following the start byte is recognized as the upper eight bits of instruction and the second byte is recognized as the lower 8 bits of instruction.

When reading data from the GRAM, valid data is not transferred to the data bus until first five bytes of data are read from the GRAM following the start byte. The R61505 sends valid data to the data bus when it reads the sixth and subsequent byte data.

Table 54 Start Byte Format

Transferred Bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: The ID bit is determined by setting the IM0/ID pin.

Table 55 Functions of RS, R/W bits

RS	R/W	Function
0	0	Set index register
0	1	Setting inhibited
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

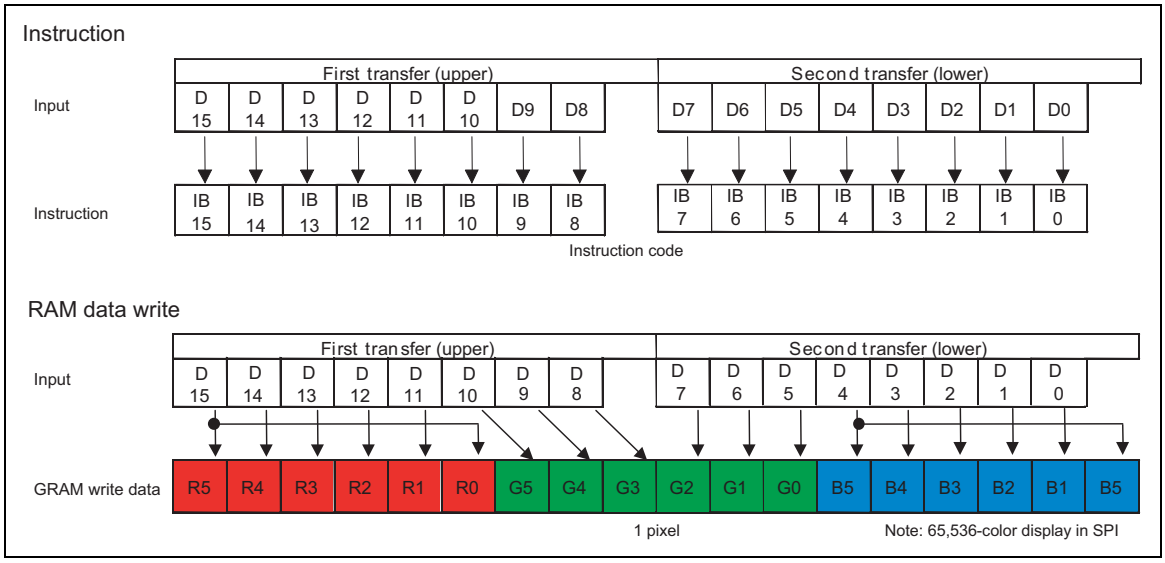


Figure 27 Serial Interface Data Format

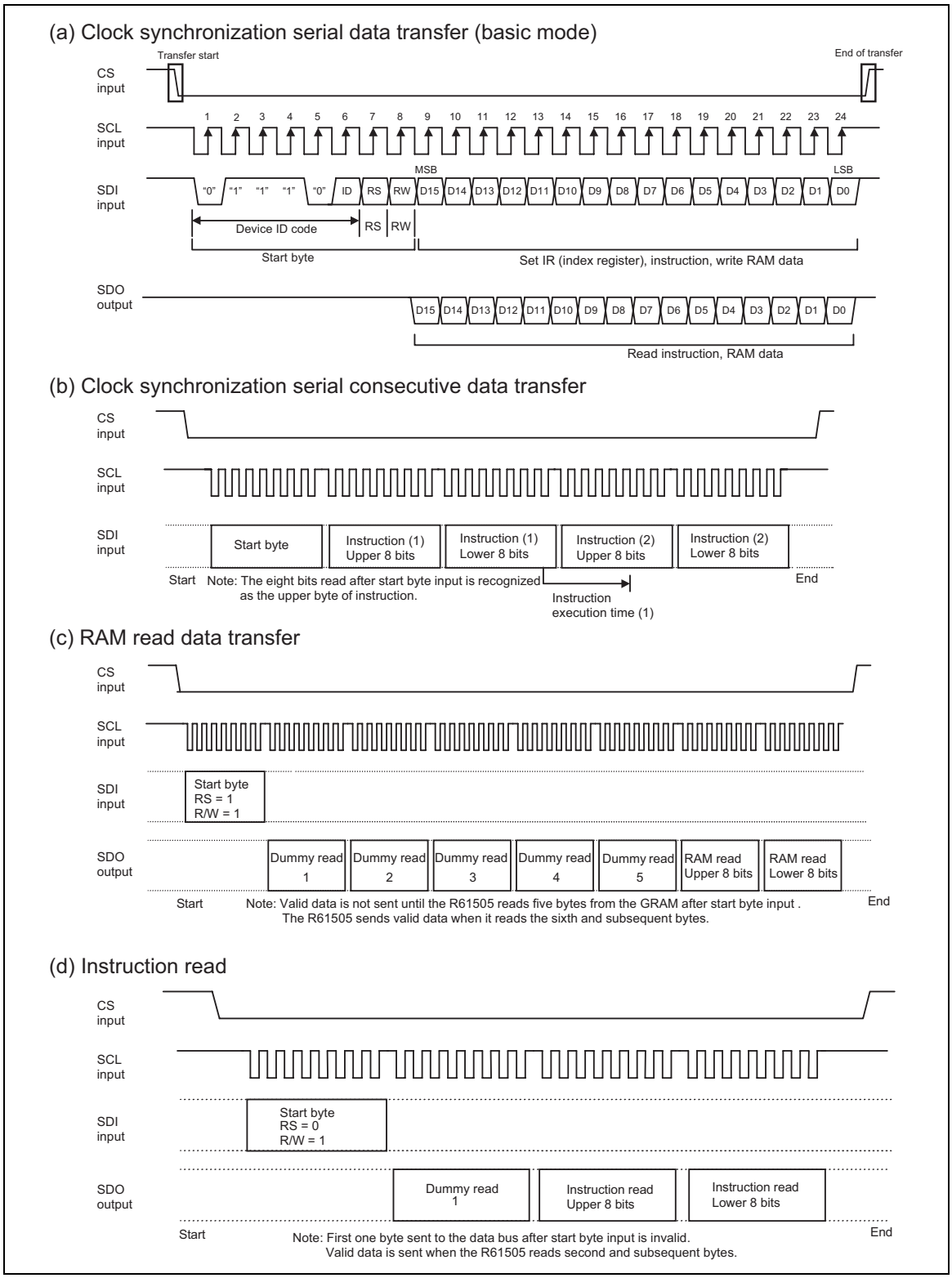


Figure 28 Data Transfer in Serial interface

VSYNC Interface

The R61505 supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation.

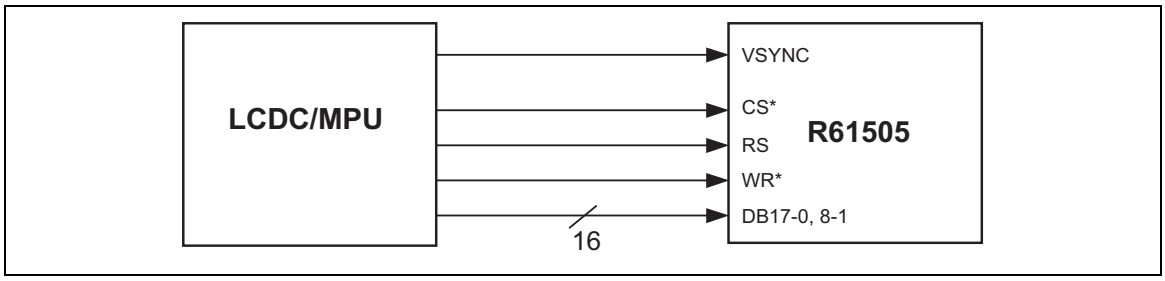


Figure 29 VSYNC Interface

The VSYNC interface is selected by setting DM1-0 = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display operation speed + margin), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the R61505 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display. By writing data using high-speed write function (HWM =1), the R61505 can write data via VSYNC interface in high speed with low power consumption.

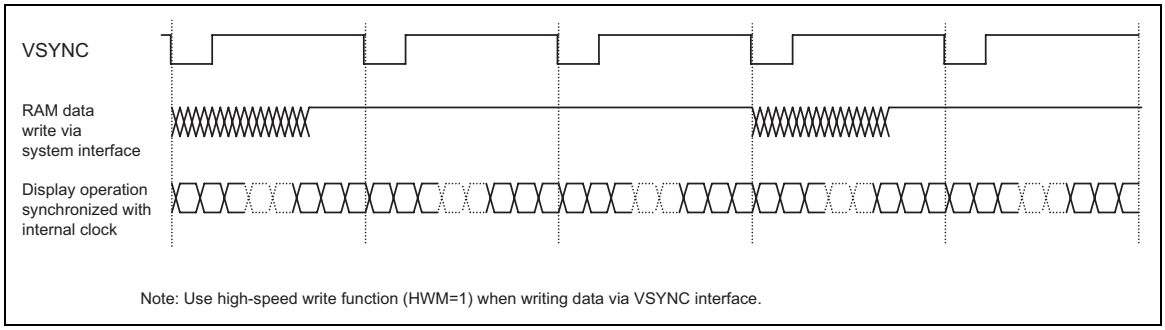


Figure 30 Moving Picture Data Transfers via VSYNC Interface

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

Internal clock frequency (fosc) [Hz]

$$= FrameFrequency \times (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) \times 16(clocks) \times \text{variance}$$

$$RAMWriteSpeed(\text{min.})[Hz] > \frac{240 \times DisplayLines(NL)}{(BackPorch(BP) + DisplayLines(NL) - \text{margins}) \times 16(clocks) \times \frac{1}{fosc}}$$

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Panel size	240 RGB × 320 lines (NL = 6'h27: 320 lines)
Total number of lines (NL)	320 lines
Back/front porch	14/2 lines (BP = 4h'E, FP = 4'h2)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz]
= 60 Hz × (320 + 2 + 14) lines × 16 clocks × 1.1 / 0.9 = 394 kHz

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one VSYNC cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz]
> 240 × 320 / {((14 + 320 - 2) lines × 16 clocks) × 1/394 kHz} = 5.7 MHz

Notes: 1. In this example, it is assumed that the R61505 starts writing data in the internal RAM on the falling edge of VSYNC.
2. There must be at least a margin of 2 lines between the line to which the R61505 has just written data and the line where display operation on the LCD is performed.

In this example, the RAM write operation at a speed of 5.7MHz or more, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the R61505 starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

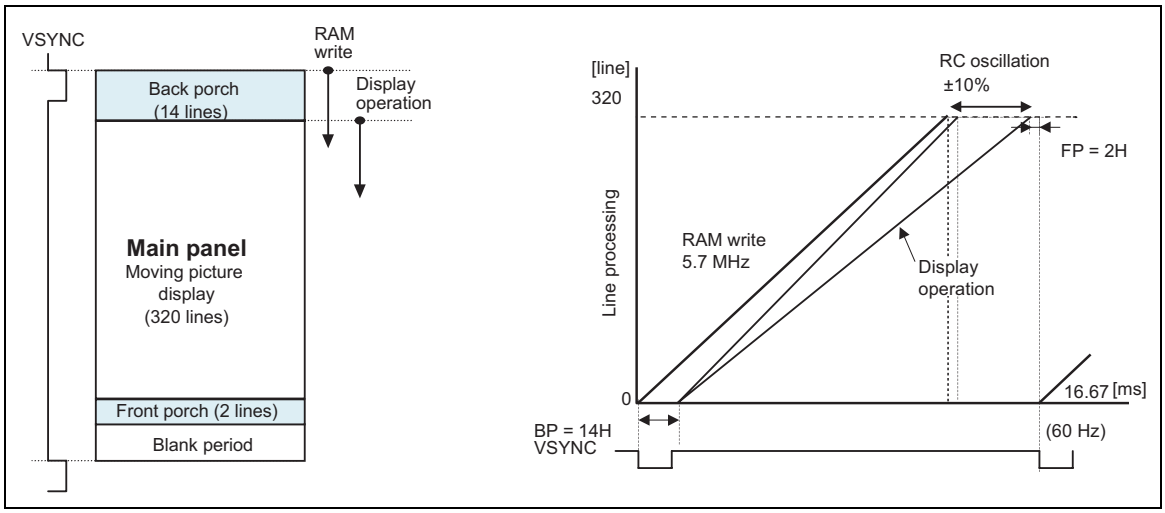


Figure 31 Write/Display Operation Timing via VSYNC Interface

Notes on VSYNC Interface Operation

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margin in setting RAM write speed for VSYNC interface operation.

2. The above example shows the values when writing over the full screen. Extra margin will be created if the moving picture display area is smaller than that.

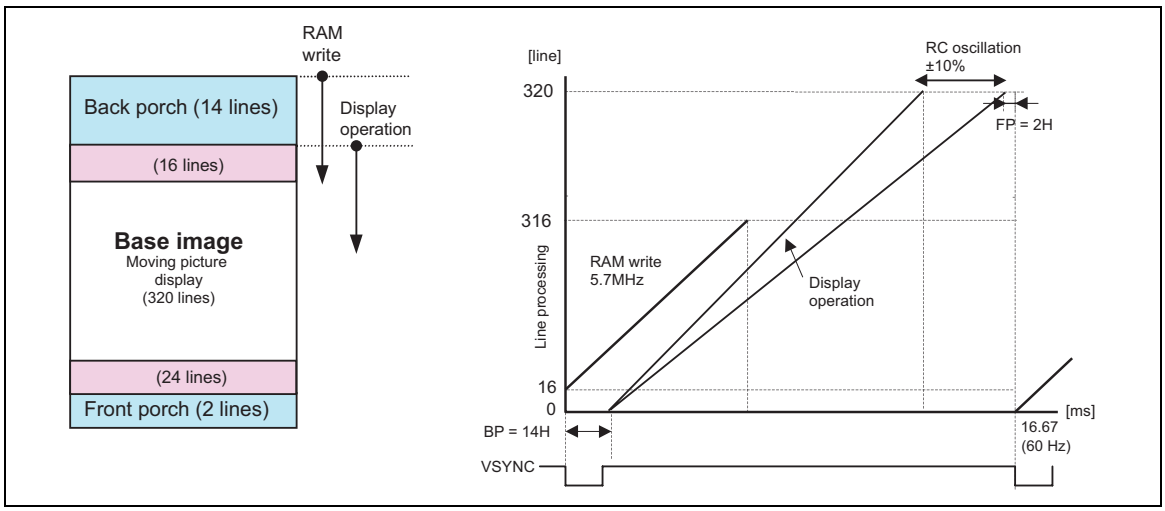


Figure 32 RAM Write Speed Margins

3. The front porch period continues from the end of one frame period to the next VSYNC input.
4. The instructions to switch from internal clock operation (DM1-0 = 00) to VSYNC interface operation modes and vice versa are enabled from the next frame period.
5. The partial display and vertical scroll functions are not available in VSYNC interface operation.
6. In VSYNC interface operation, set AM = 0 to transfer display data correctly.
7. In VSYNC interface operation, use high-speed write function (HWM = 1) when writing display data to the internal RAM.

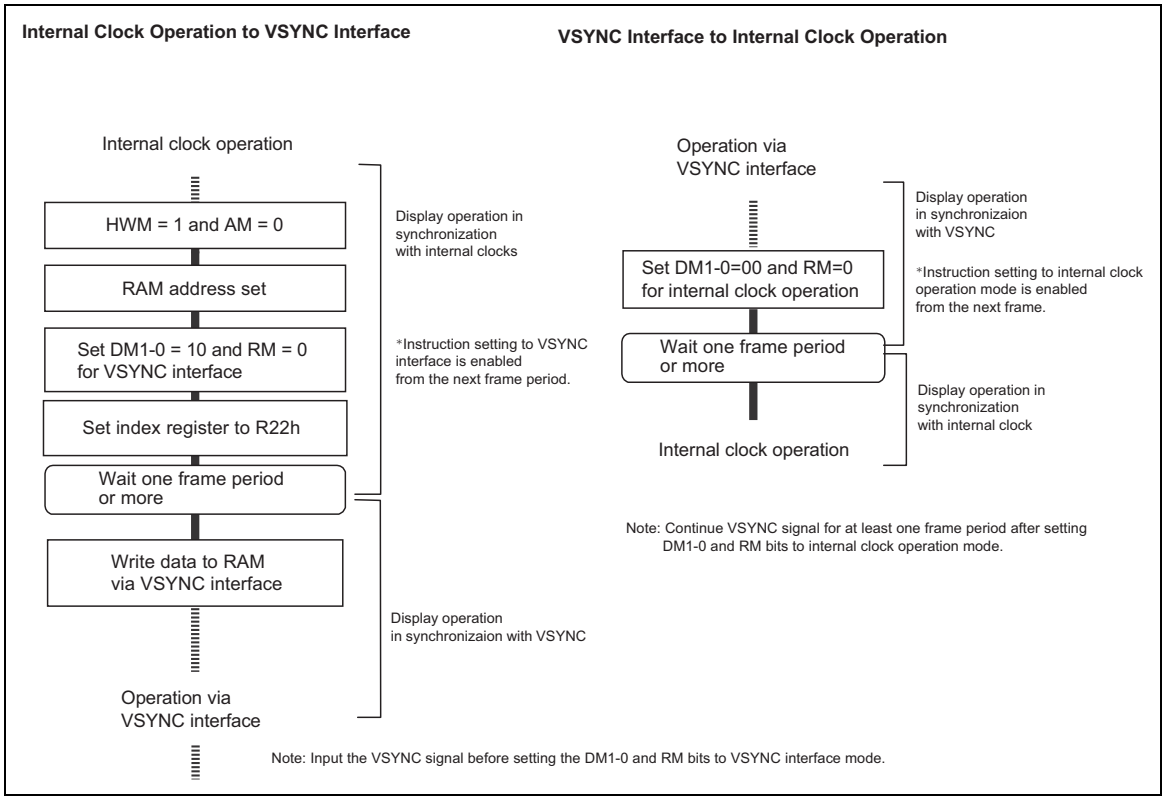


Figure 33 Sequences to Switch between VSYNC and Internal Clock Operation Modes

External Display Interface

The R61505 supports the RGB interface. The interface format is set by RM[1:0] bits. The internal RAM is accessible via RGB interface.

Table 56 RGB Interface

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, DB11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting inhibited	-

Note: Using multiple interface at a time is prohibited.

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The data can be written only within the specified area with low power consumption by using window address function and high-speed write mode (HWM = 1). In RGB interface operation, front and back porch periods must be made before and after the display period.

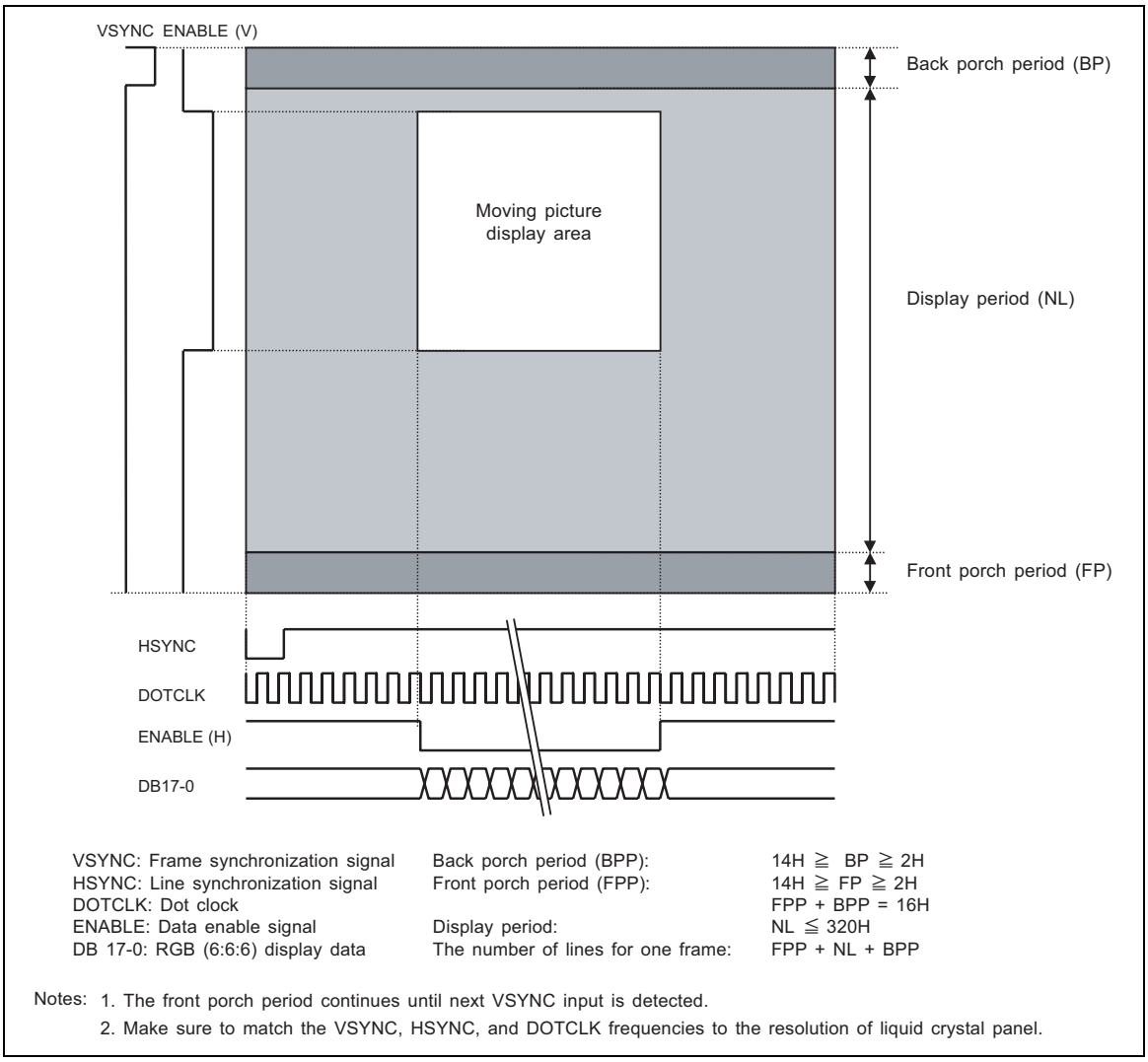


Figure 34 Display Operation via RGB Interface

Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals can be changed by setting the DPL, EPL, HSPL, and VSPL bits, respectively for convenience of system configuration.

RGB Interface Timing

The timing relationship of signals in RGB interface operation is as follows.

16-/18-Bit RGB Interface Timing

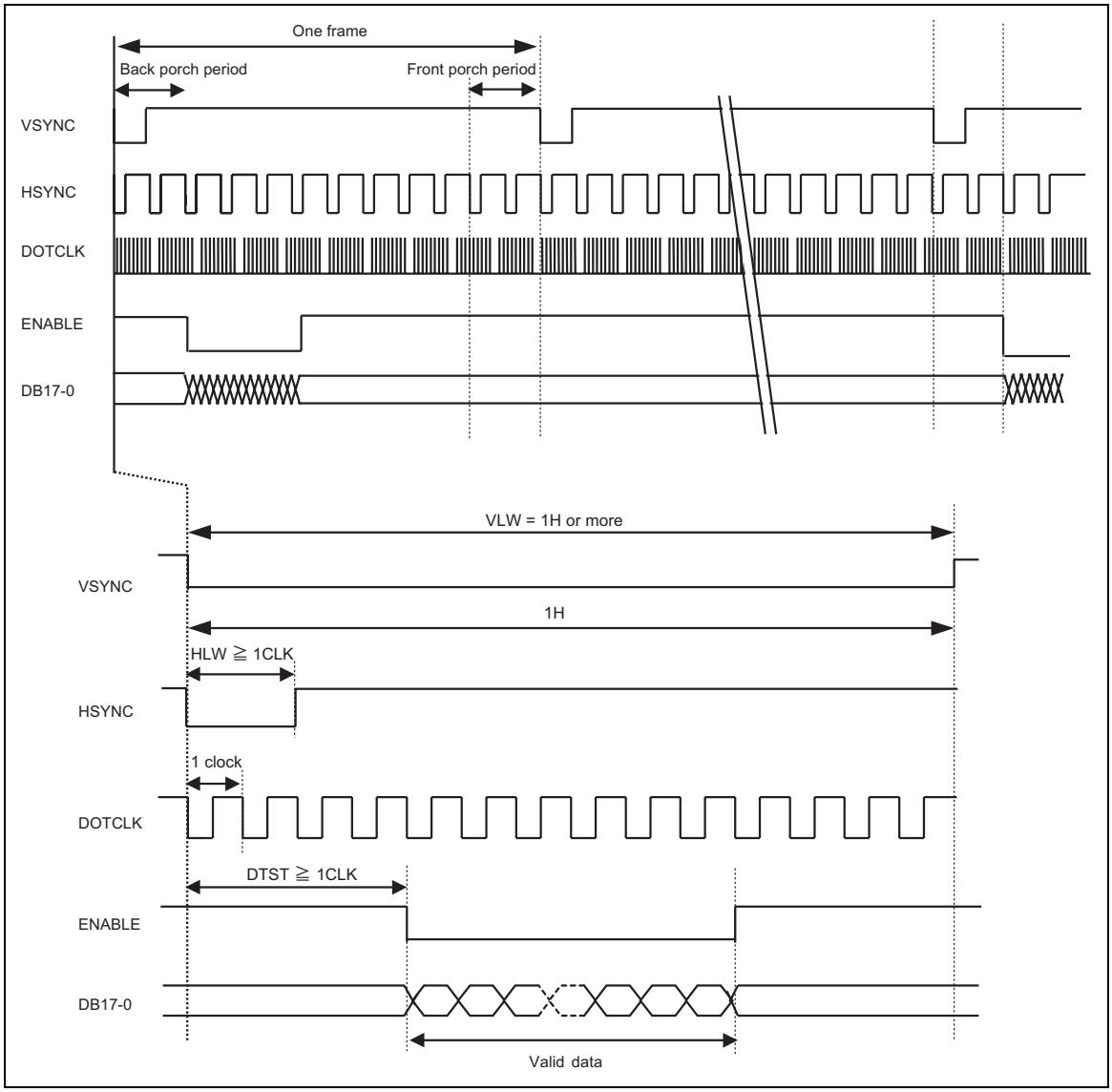


Figure 35

Notes: 1. VLW: VSYNC Low period
HLW: HSYNC Low period
DTST: data transfer setup time
2. Use high-speed write function (HWM = 1) when writing data via RGB interface.

6-Bit RGB Interface Timing

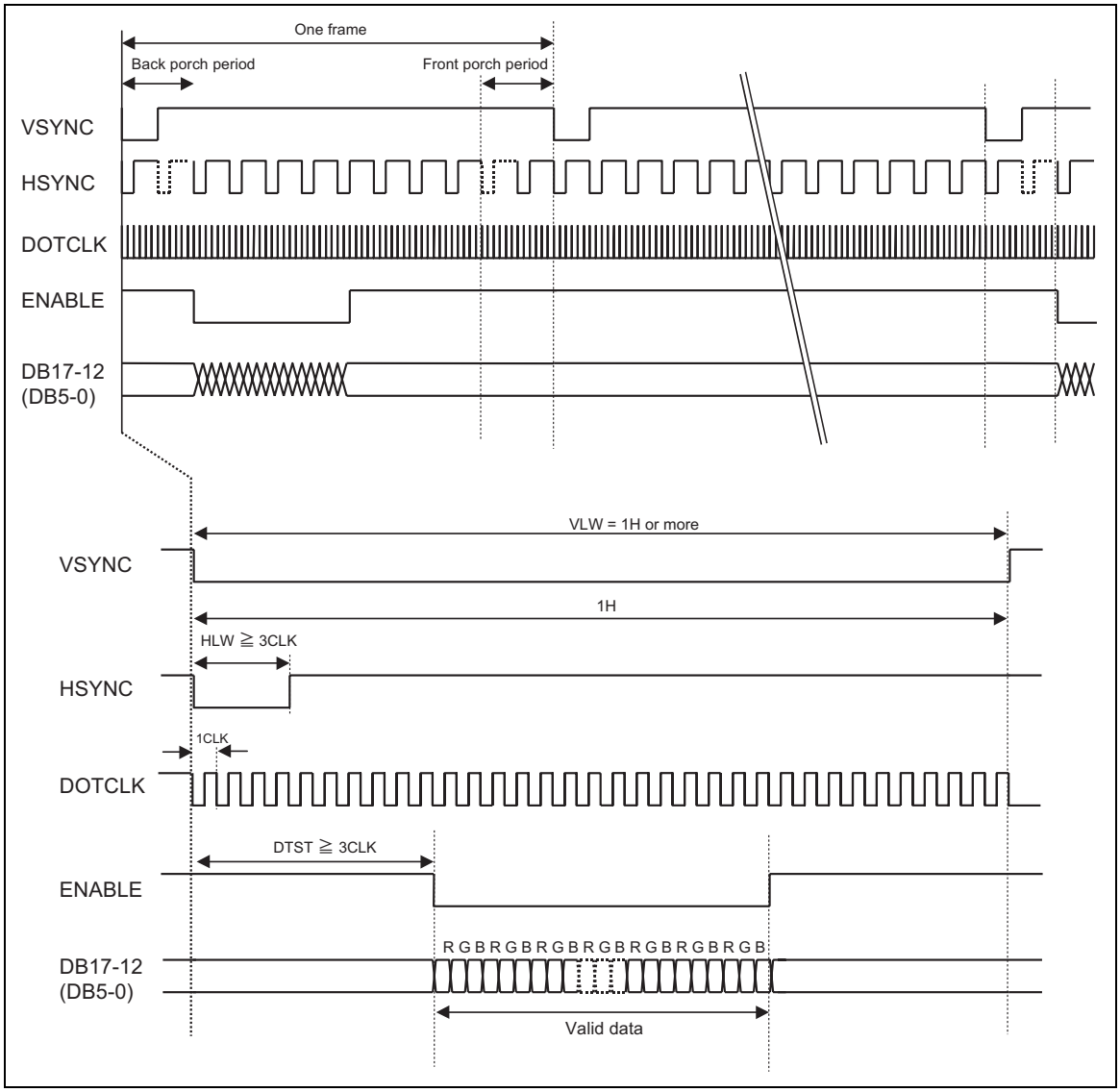


Figure 36

Notes: 1. VLW: VSYNC Low period
HLW: HSYNC Low period
DTST: Data transfer setup time
2. Use high-speed write function (HWM = 1) when writing data via RGB interface.
3. In 6-bit RGB interface operation, set the VSYNC, HSYNC, ENABLE, DOTCLK cycles so that one pixel is transferred in units of three DOTCLKs via DB17-12 (DB5-0).

Moving Picture Display via RGB Interface

The R61505 supports RGB interface for moving picture display and incorporates RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function enables transferring data only within the moving picture area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. It becomes possible to transfer only the data written over the moving picture area
4. By reducing data transfer, it can contribute to lowering the power consumption of the whole system
5. The data in still picture area (icons etc.) can be written over via system interface while displaying a moving picture via RGB interface

RAM Access via System Interface in RGB Interface Operation

The R61505 allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is "Low". When writing data to the RAM via system interface, set ENABLE "High" to stop writing data via RGB interface. Then set RM = "0" to enable RAM access via system interface. When reverting to the RGB interface operation, wait for the read/write bus cycle time. Then, set RM = "1" and the index register to R22h to start accessing RAM via RGB interface. If there is a conflict between RAM accesses via two interfaces, there is no guarantee that the data is written in the RAM.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

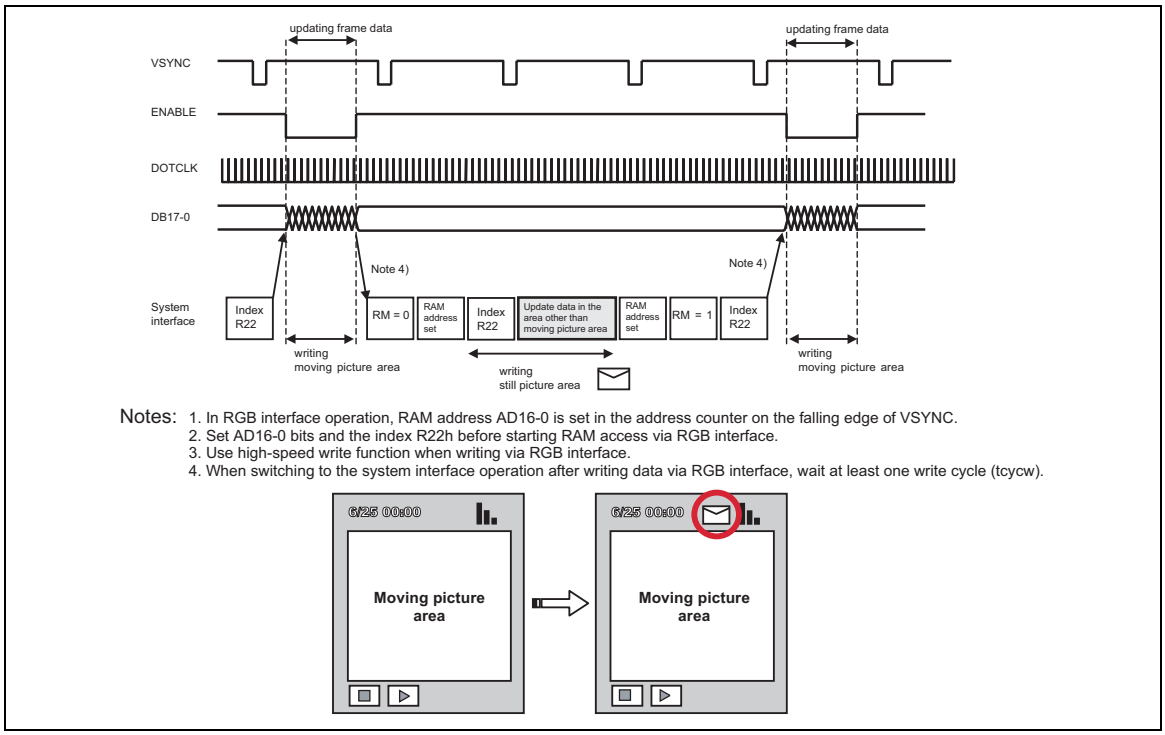


Figure 37 Updating the Still Picture Area while Displaying Moving Picture

6-Bit RGB Interface

The 6-bit RGB interface is selected by setting RIM1-0 = 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit port while data enable signal (ENABLE) allows RAM access via RGB interface. Unused pins DB11-0 (DB17-6) must be fixed at either IOVcc or IOGND level.

Instruction bits can be transferred only via system interface.

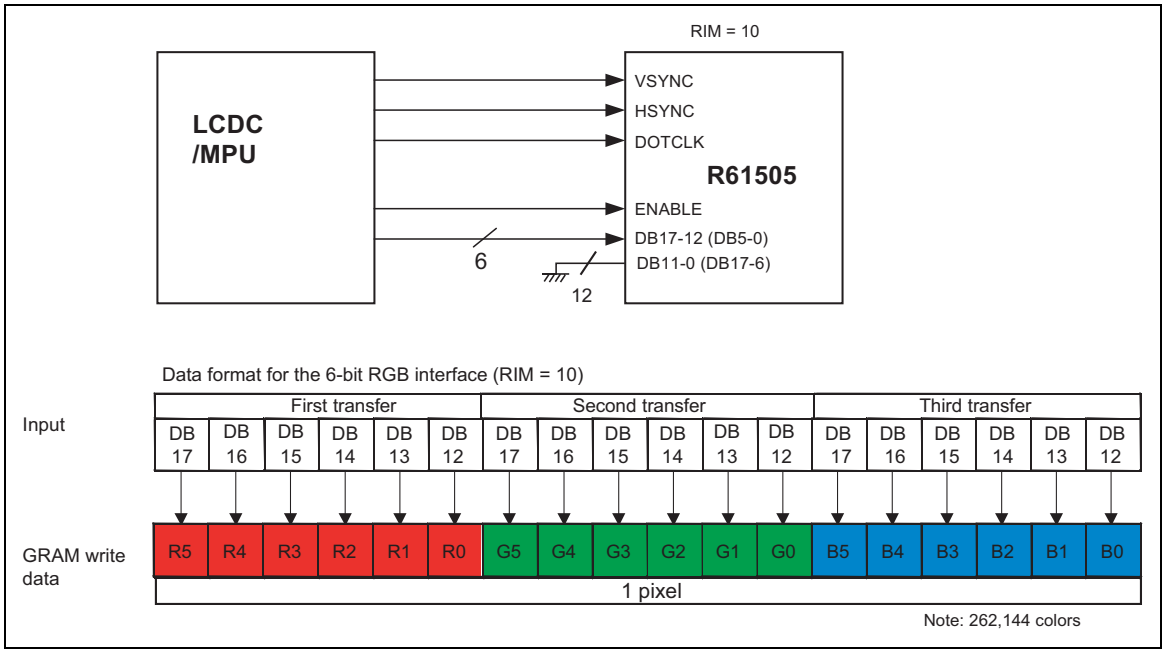


Figure 38 Example of 6-Bit RGB Interface and Data Format

Data Transfer Synchronization in 6-Bit Bus Interface Operation

The R61505 has the counters, which count the first, second, third 6 bit transfers via 6-bit RBG interface. The counters are reset on the falling edge of VSYNC so that the data transfer will start from the first 6 bits of 18-bit RGB data from the next frame period. Accordingly, the data transfer via 6-bit interface can restart in correct order from the next frame period even if a mismatch occurs in transferring 6-bit data. This function can minimizes the effect from data transfer mismatch and help the display system return to normal display operation when data is transferred consecutively in moving picture operation.

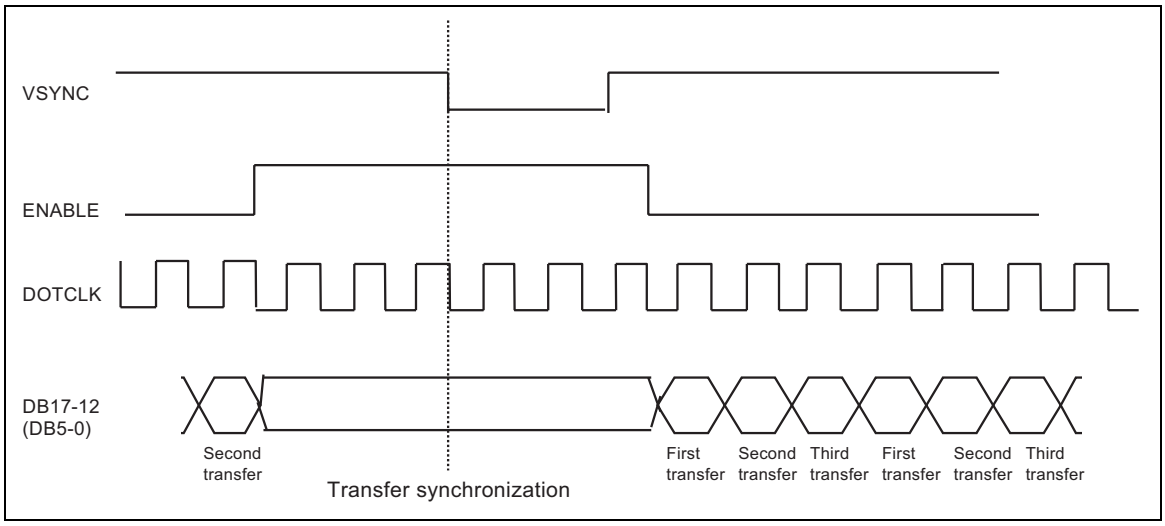


Figure 39 6-Bit Transfer Synchronization

16-Bit RGB interface

The 16-bit RGB interface is selected by setting RIM1-0 = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit ports while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

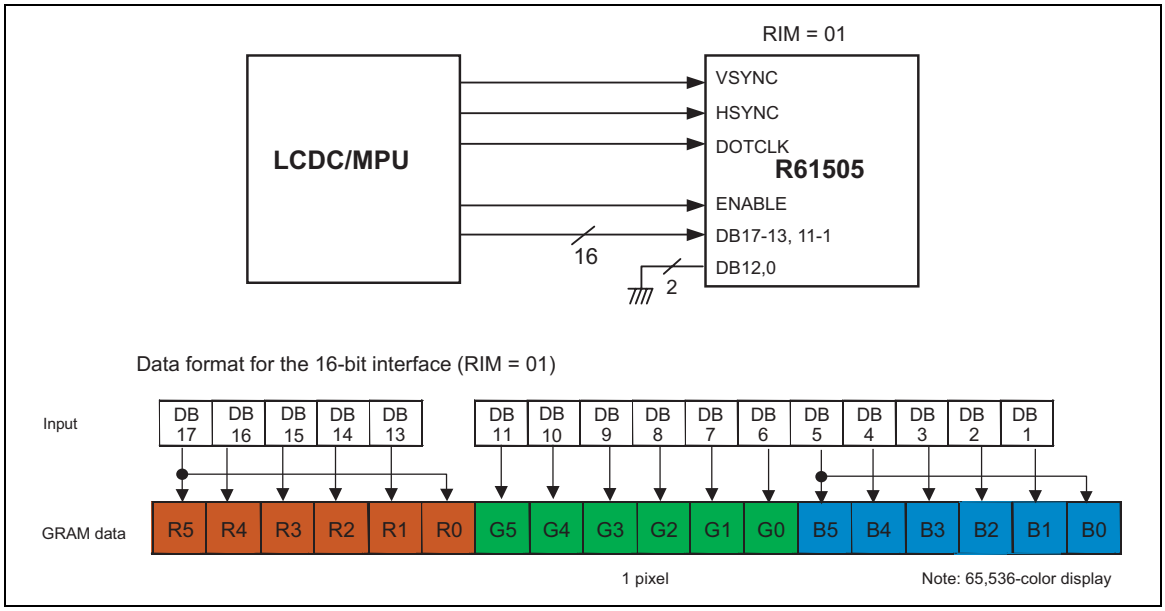


Figure 40 Example of 16-Bit RGB Interface and Data Format

18-Bit RGB interface

The 18-bit RGB interface is selected by setting RIM1-0 = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit ports (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

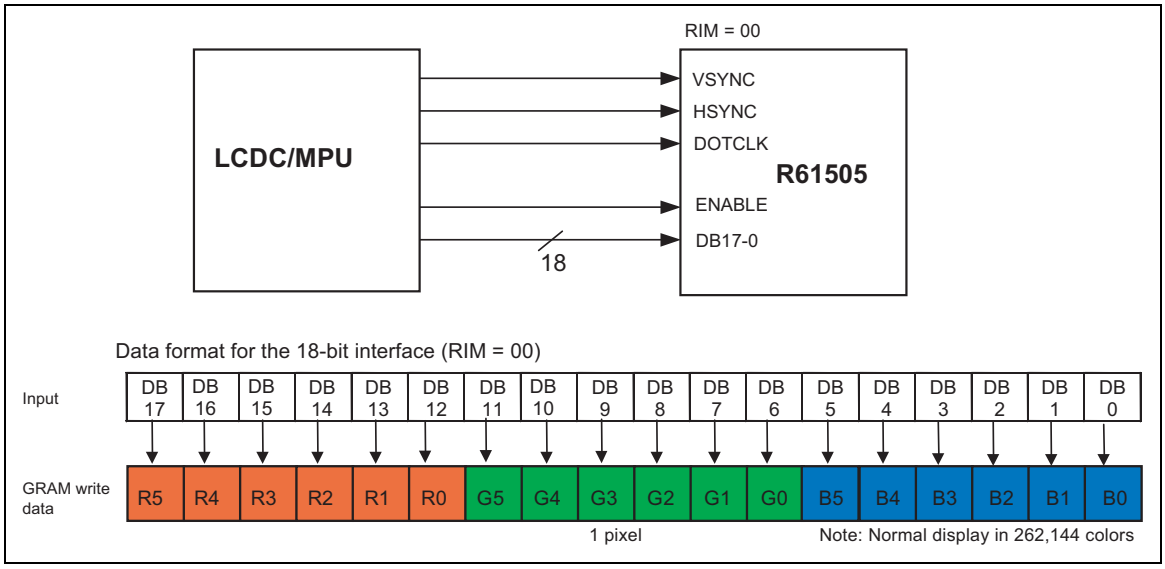


Figure 41 Example of 18-Bit RGB Interface and Data Format

Notes on External Display Interface Operation

1. The following functions are not available in external display interface operation.

Table 57 Functions Not Available in External Display Interface Operation

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.
3. The reference clock to generate liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.
4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel data.
5. In 6-bit RGB interface operation, make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE signals so that the data transfer is completed in units of pixels.
6. When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.
7. In RGB interface operation, front porch period continues after the end of frame period until next VSYNC input is detected.
8. In RGB interface operation, use high-speed write function (HWM = 1) when writing data to the internal RAM.
9. In RGB interface operation, RAM address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

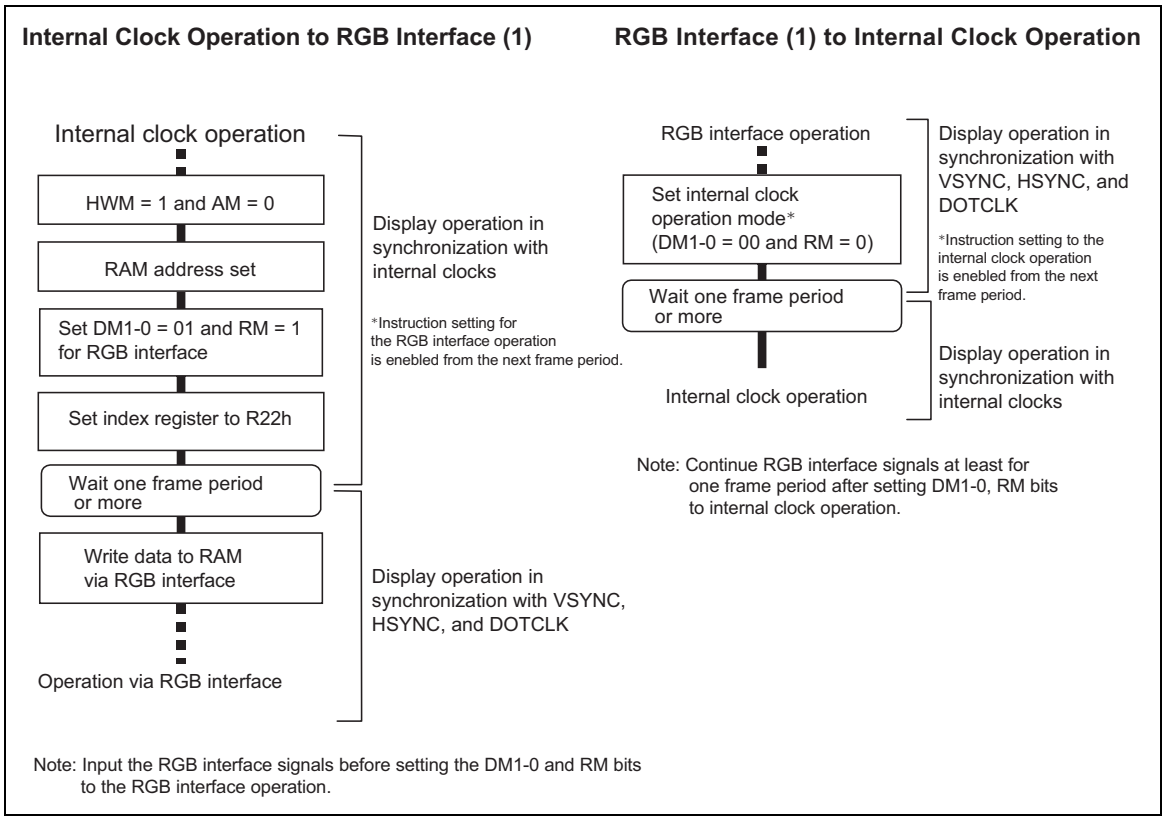


Figure 42 RGB and Internal Clock Operation Mode Switching Sequences

RAM Address and Display Position on the Panel

The R61505 has memory to store display data of 240RGB x 320 lines. The R61505 incorporates a circuit to control partial display, which allows switching driving method between full-screen display mode and partial display mode.

The R61505 makes display arrangement setting and panel driving position control setting separately and specifies RAM area for each image displayed on the panel. For this reason, there is no need to take the mounting position of the panel into consideration when designing a display on the panel.

The following is the sequence of setting full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image by setting PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

Normal display	BASEE = 1
Partial display 1/2	BASEE = 0, PTDE0/1 = 1

5. Changes BASEE, PTDE0/1 settings when turning on and off the full and partial displays 1/2.

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, set SS bit when writing RAM data.

Table 58

	Display ENABLE	Numbers of lines	RAM Area
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h13F)

Notes 1: The base image is displayed from the first line of the screen.

2: Make sure NL ≤ 320 (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h13F, respectively.

Table 59

	Display ENABLE	Display Position	RAM Area
Partial Image 1	PTDE0	PTDP0	(PTSA0, PTEA0)
Partial Image 2	PTDE1	PTDP1	(PTSA1, PTEA1)

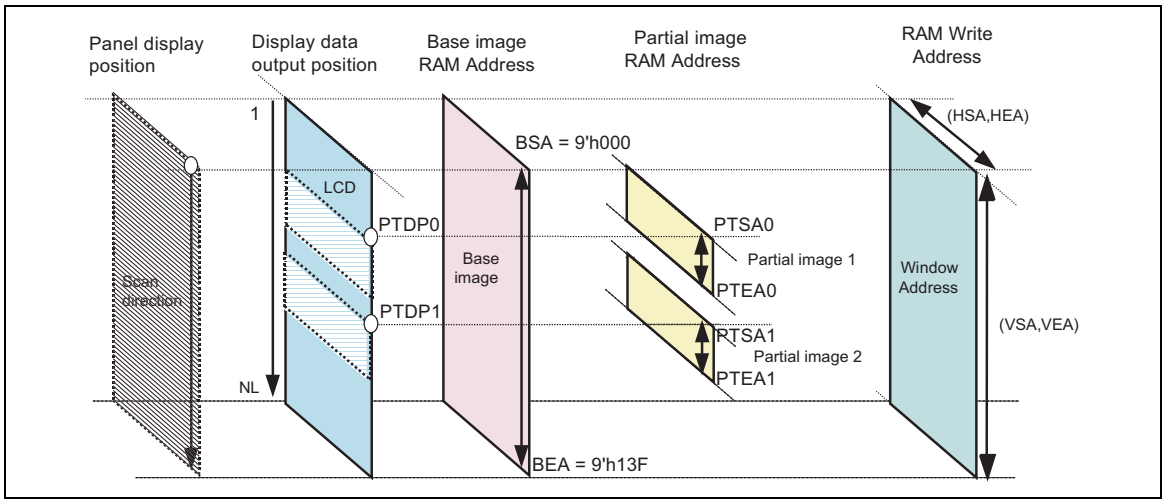


Figure 43 RAM Address, Display Position and Drive Position

Restrictions in Setting Display Control Instruction

There are restrictions in coordinates setting for display data, display position and partial display.

Screen Setting

In setting the number of lines to drive the liquid crystal panel, make sure that the total number of lines is 320 lines or less (NL ≤ 320 lines).

Base Image Display

1. The base image is displayed from the first line of the screen: BSA = 1st line (of the display panel)
2. The base image RAM area (specified by BSA = 000, BEA = 13F) must include the same or more number of lines set by NL bits (liquid crystal panel drive lines): BEA – BSA = 320 lines ≥ NL

Partial Image Display

Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partial images do not overlap one another.

$$0 \le PTDP0 \le PTDP0 + (PTEA0 - PTSA0) < PTDP1 \le PTDP1 + (PTEA1 - PTSA1) \le NL$$

The following figure shows the relationship among the RAM address, display position, and the lines driven for the display.

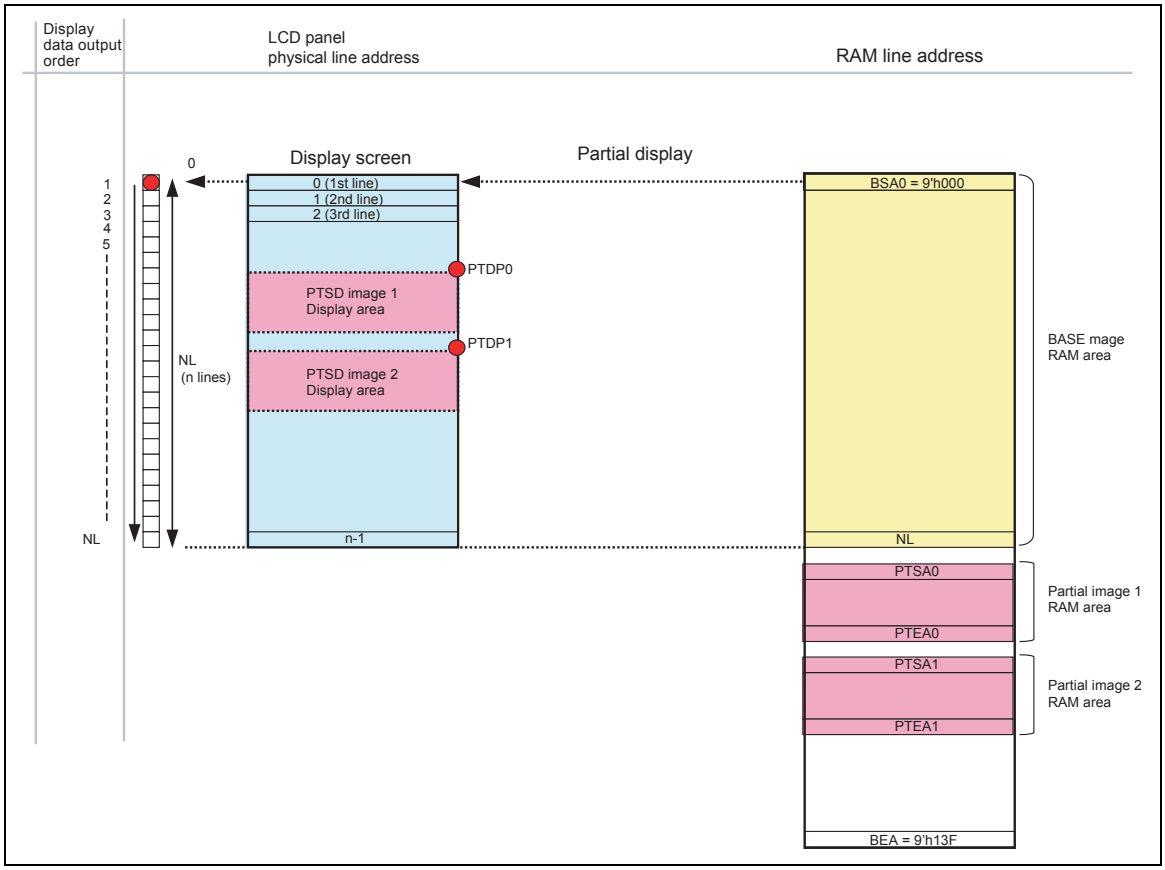


Figure 44 Display RAM Address and Panel Display Position

Note: This figure shows the relationship between RAM line address and the display position on the panel. In the R61505's internal operation, the data is written in the RAM area specified by the window address setting (R50h~R53h).

Instruction Setting Example

The followings are examples of settings for 240(RGB) x 320(lines) panel.

1. Full Screen Display (No Partial Display)

The following is an example of settings for full screen display.

Table 60

Base Image Display Instruction	
BASEE	1
NL[5:0]	6'h27

PTDE0	0
PTDE1	0

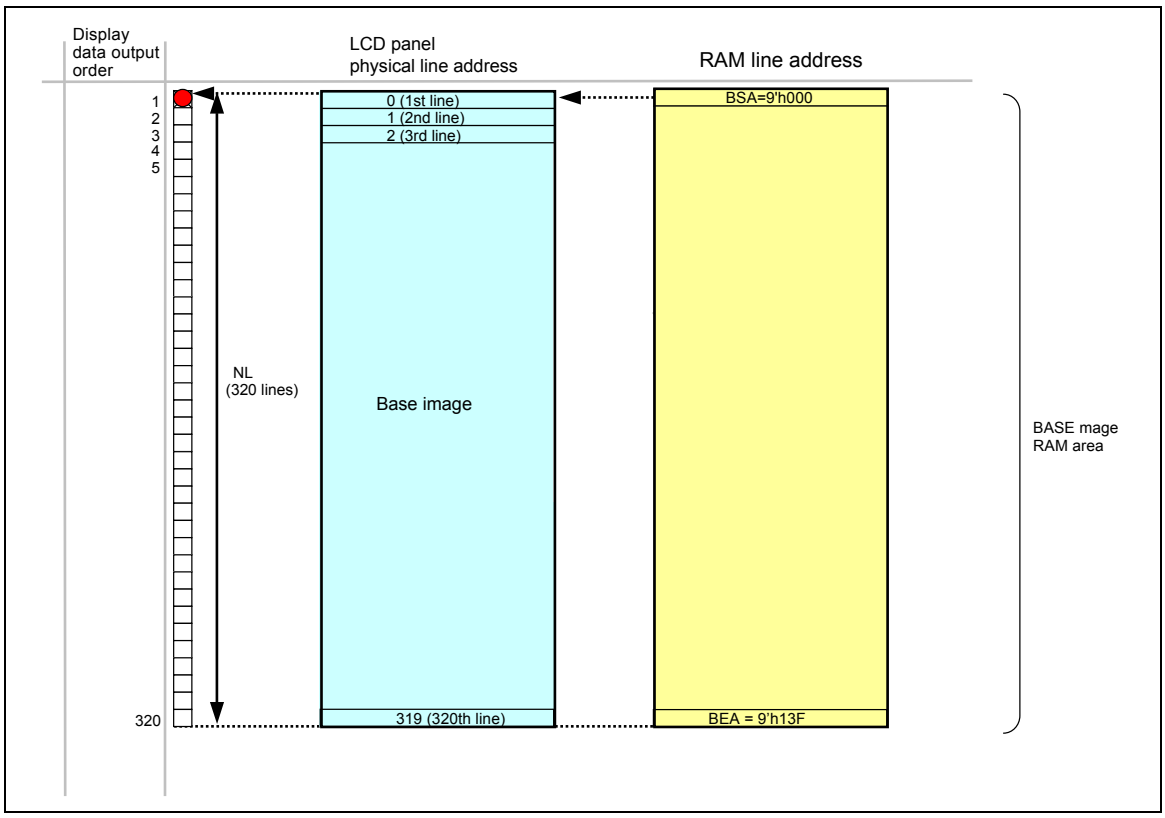


Figure 45 Full Screen Display (No Partial)

2. Partial Only

The following is an example of settings for displaying partial image 1 only and turning off the base image. The partial image 1 is displayed at the position specified by PTDP0 bit.

Table 61

Base Image Display Instruction	
BASEE	0
NL[5:0]	6'h27

Partial Image 1 Display Instruction	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080

Partial Image 2 Display Instruction	
PTDE1	0
PTSA1[8:0]	9'h000
PTEA1[8:0]	9'h000
PTDP1[8:0]	9'h000

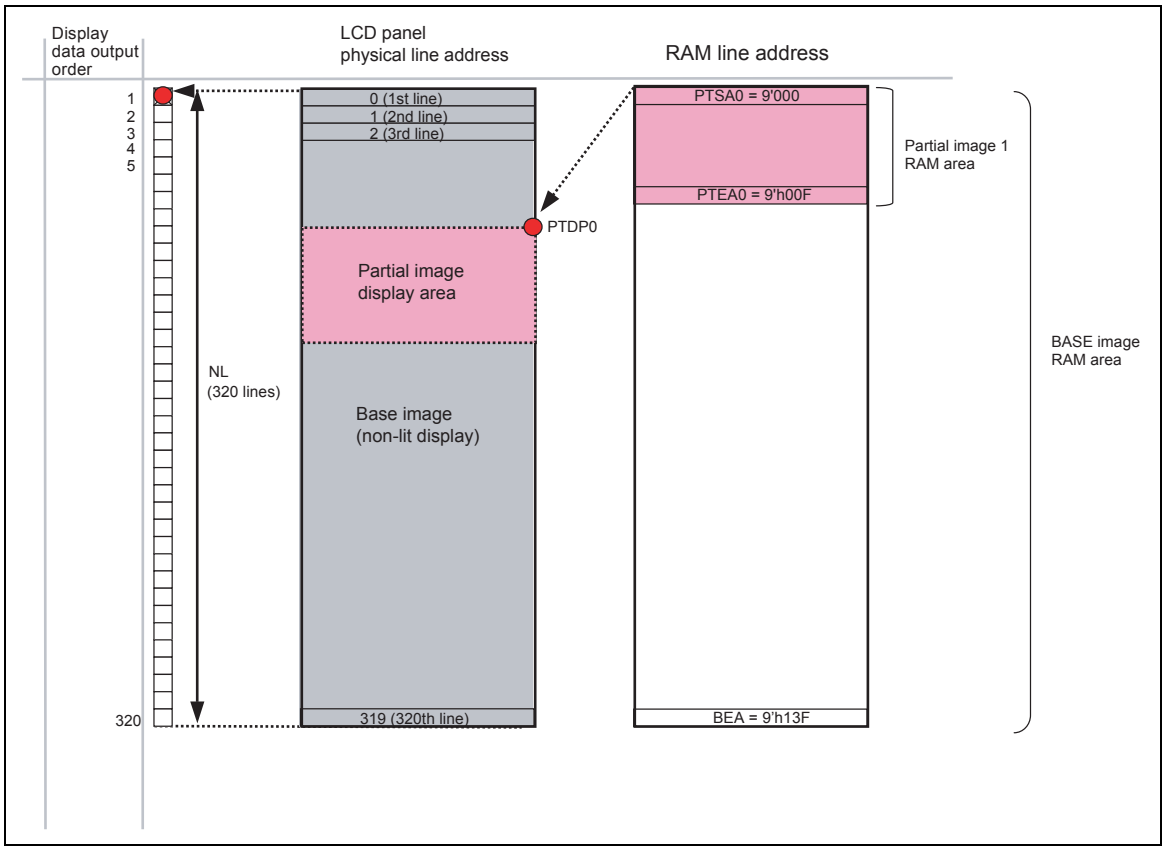


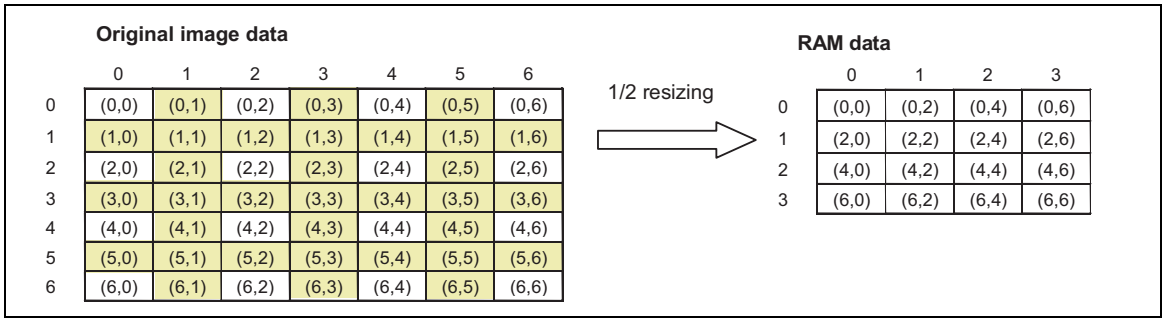
Figure 46 Partial Display

Resizing Function

The R61505 supports resizing function (x 1/2, x 1/4), which is performed when writing image data. The resizing function is enabled by setting a window address area and the RSZ bit representing the contraction factor (x1/2 or x1/4) of the image. This function enables the R61505 to write the resized image data directly to the internal RAM, while allowing the system to transfer the original-sized image data.

The resizing function allows the system to transfer data as usual even when resizing of the image is required. This feature makes image resizing easily available with various applications such as camera display, sub panel display, thumbnail display and so on.

The R61505 processes the contraction of an image simply by selecting pixels. For this reason, the resized image may appear distorted when compared with the original image. Check the resized image before use.



	0	1	2	3	4	5	6
0	(0,0)	(0,1)	(0,2)	(0,3)	(0,4)	(0,5)	(0,6)
1	(1,0)	(1,1)	(1,2)	(1,3)	(1,4)	(1,5)	(1,6)
2	(2,0)	(2,1)	(2,2)	(2,3)	(2,4)	(2,5)	(2,6)
3	(3,0)	(3,1)	(3,2)	(3,3)	(3,4)	(3,5)	(3,6)
4	(4,0)	(4,1)	(4,2)	(4,3)	(4,4)	(4,5)	(4,6)
5	(5,0)	(5,1)	(5,2)	(5,3)	(5,4)	(5,5)	(5,6)
6	(6,0)	(6,1)	(6,2)	(6,3)	(6,4)	(6,5)	(6,6)

	0	1	2	3
0	(0,0)	(0,2)	(0,4)	(0,6)
1	(2,0)	(2,2)	(2,4)	(2,6)
2	(4,0)	(4,2)	(4,4)	(4,6)
3	(6,0)	(6,2)	(6,4)	(6,6)

Figure 47 Data Transfer in Resizing

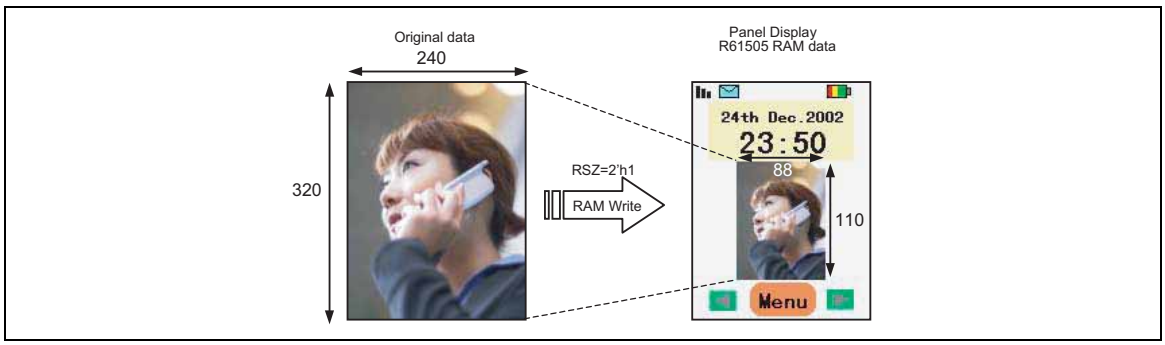


Figure 48 Data Transfer, Display Example in Resizing

Table 62

Original Image Size (X x Y)	Resized Image Size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
640x480(VGA)	320x240	160x120
352x288 (CIF)	176x144	88x72
320x240 (QVGA)	160x120	80x60
176x144 (QCIF)	88x72	44x36
120x160	60x80	30x40
132x176	66x88	33x44

Resizing Setting

The RSZ bit sets the resizing (contraction) factor of an image. When setting a window address area in the internal RAM, the window address area must fit the size of the resized picture. If there are surplus pixels as a result of resizing, which are calculated from the following equations, set RCV, RCH bits to the number of surplus pixels before writing data to the internal RAM.

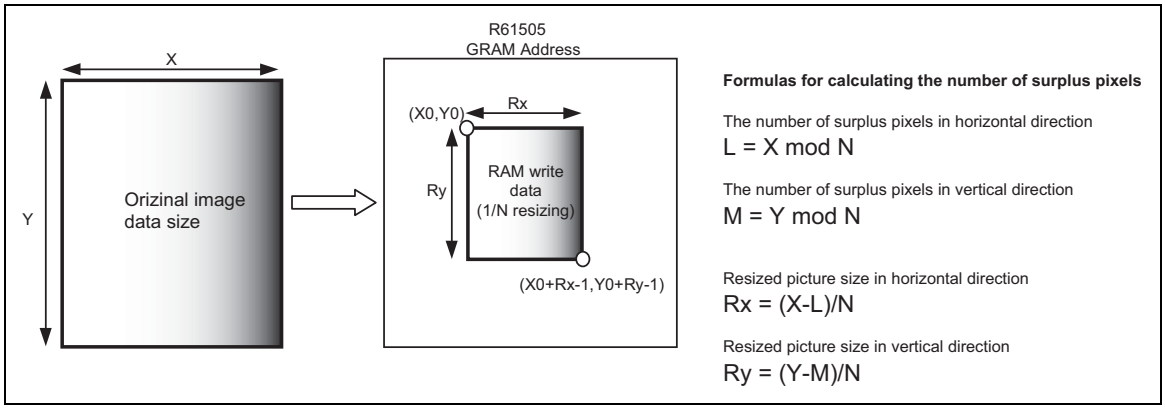


Figure 49 Resizing Setting, Surplus Pixel Calculation

Table 63

Image (before Resizing)

Number of data in horizontal direction	X
Number of data in vertical direction	Y
Resizing ratio	1/N

Register Setting in the R61505

Resizing setting	RSZ	N-1
Number of data in horizontal direction	RCV	L
Number of data in vertical direction	RCH	M

RAM writing start address	AD	(X0, Y0)
RAM window address	HSA	X0
	HEA	X0+Rx - 1
	VSA	Y0
	VEA	Y0+Ry - 1

Example of 1/2 Resizing

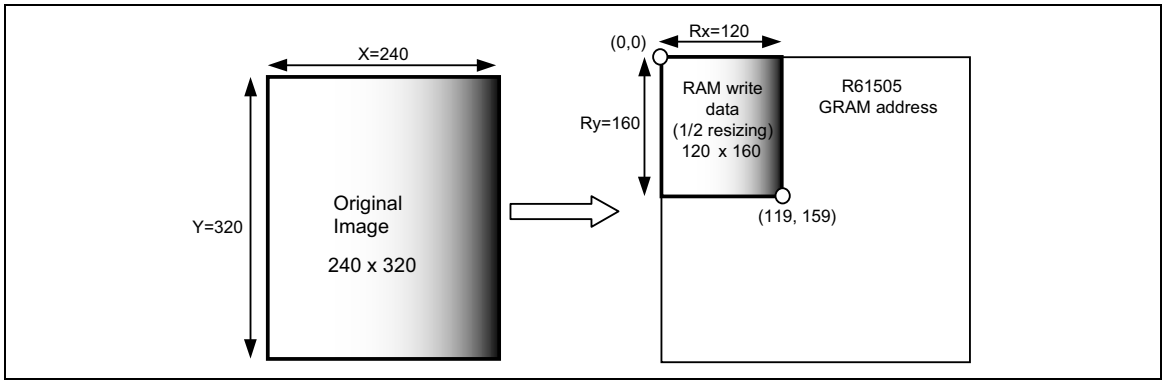


Figure 50 Example of Resizing Setting (x 1/2)

Table 64

Original Image (before Resizing)

Number of data in horizontal direction	X	240
Number of data in vertical direction	Y	320
Resizing ratio	1/N	1/2

Register Setting in the R61505

Resizing setting	RSZ	2'h1
Number of data in horizontal direction	RCV	2'h0
Number of data in vertical direction	RCH	2'h0

RAM writing start address	AD	17'h00000
RAM window address	HSA	8'h00
	HEA	8'h77
	VSA	8'h00
	VEA	8'h9F

Resizing Instruction

Table 65 Resizing Factor

RSZ[1:0]	Contraction Factor
2h'0	No resizing (x 1)
2h'1	1/2 resizing (x 1/2)
2h'2	Setting disabled
2h'3	1/4 resizing (x 1/4)
2h'4	Setting disabled

Table 66 Surplus Pixels

Vertical Direction

RCV[1:0]	Surplus pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

1 pixel = 1 RGB

horizontal Direction

RCH[1:0]	Surplus Pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

1 pixel = 1 RGB

Notes on Resizing Function

1. Set the resizing instruction bits (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 (R20h, R21h) before start transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are surplus pixels. Otherwise (if RSZ = 2'h0), set RCH = RCV = 2'h0.

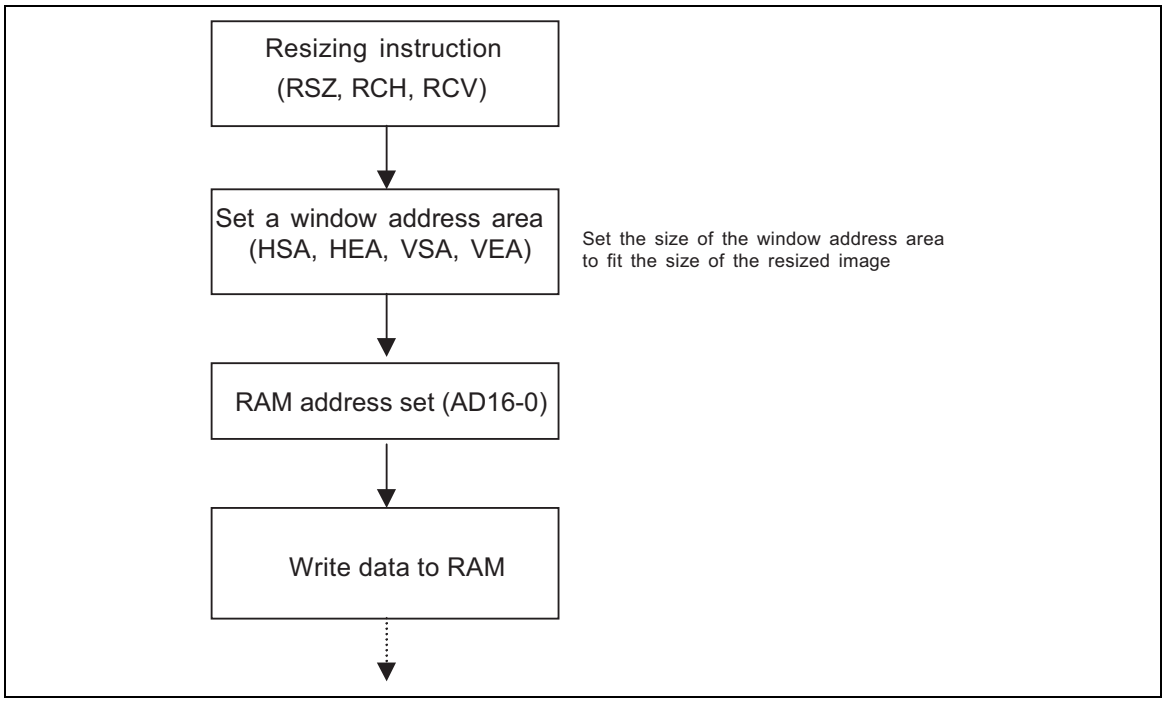


Figure 51 RAM Write Operation Sequence in Resizing

FMARK Function

The R61505 outputs an FMARK pulse when the R61505 is driving the line specified by FMP[8:0] bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

The FMARK output interval is set by FMI[2:0] bits. Set FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. Set FMARKOE = 1 when outputting FMARK pulse from the FMARK pin.

Table 67

FMP[8:0]	FMARK Output Position
9'h000	0
9'h001	1st line
9'h002	2nd line
:	:
9'h14D	333rd line
9'h14E	334th line
9'h14F	335th line
9'h150 ~ 1FF	Setting disabled

Table 68

FMI[2]	FMI[1]	FMI[0]	FMARK Output Interval
0	0	0	One frame period
0	0	1	2 frame periods
0	1	1	4 frame periods
1	0	1	6 frame periods
Other setting			Setting disabled

Example of FMP Setting

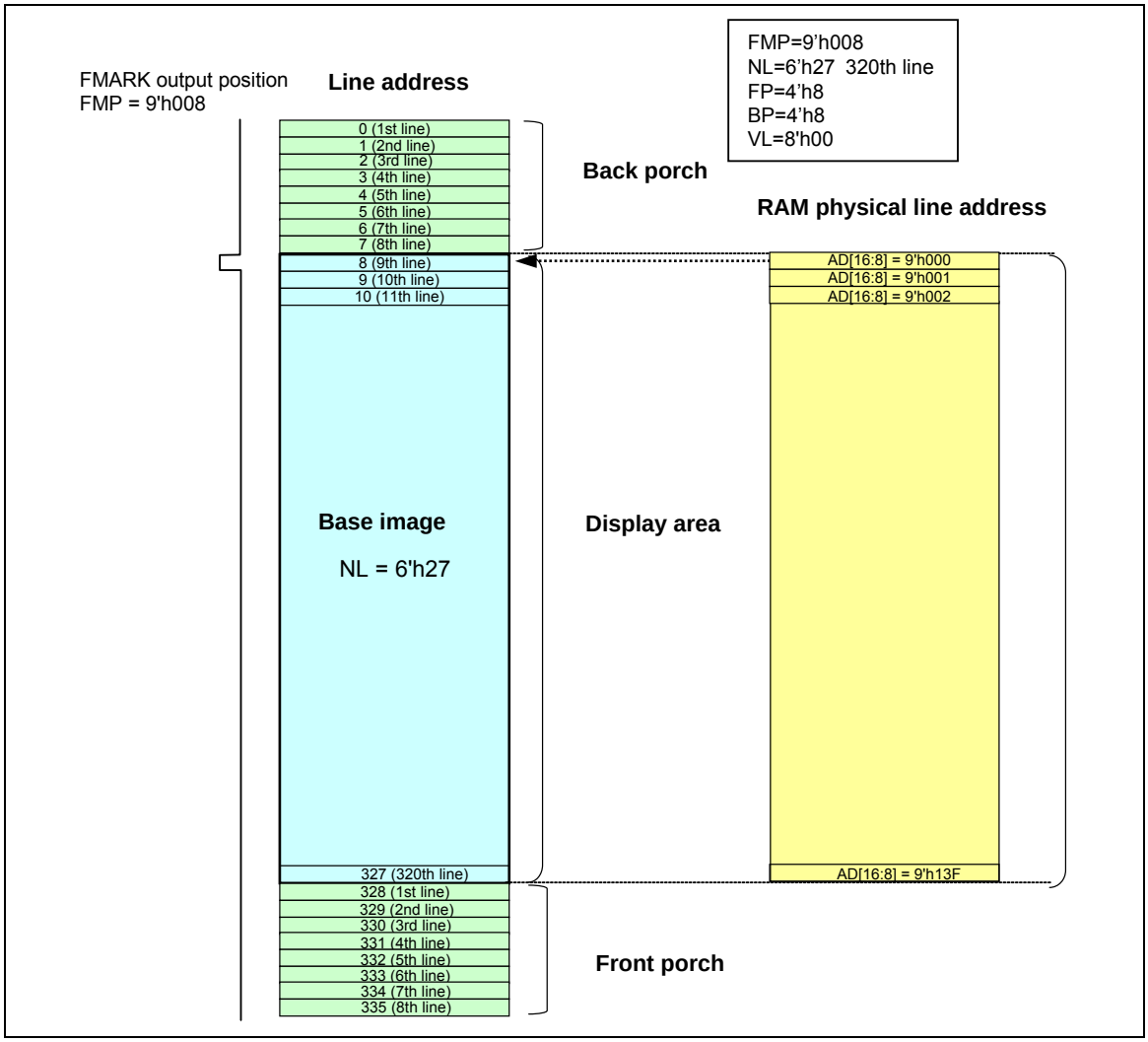


Figure 52

Display Operation Synchronous Data Transfer Using FMARK

The R61505 uses FMARK signal as a trigger signal to start writing data to the internal GRAM in synchronization with display scan operation.

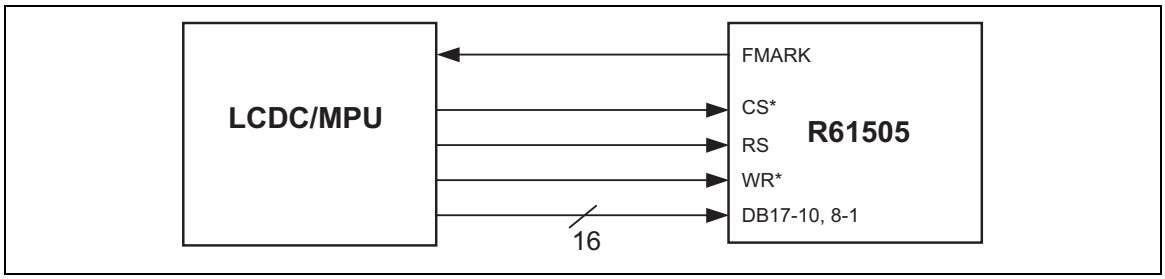


Figure 53 Display Synchronous Data Transfer Interface

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture RAM area without causing flicker on the display. The data is written in the internal RAM in order to transfer only the data written over the moving picture display area and minimize the data transfer required for moving picture display. High-speed write function (HWM = 1) enables writing data in high speed with low power consumption.

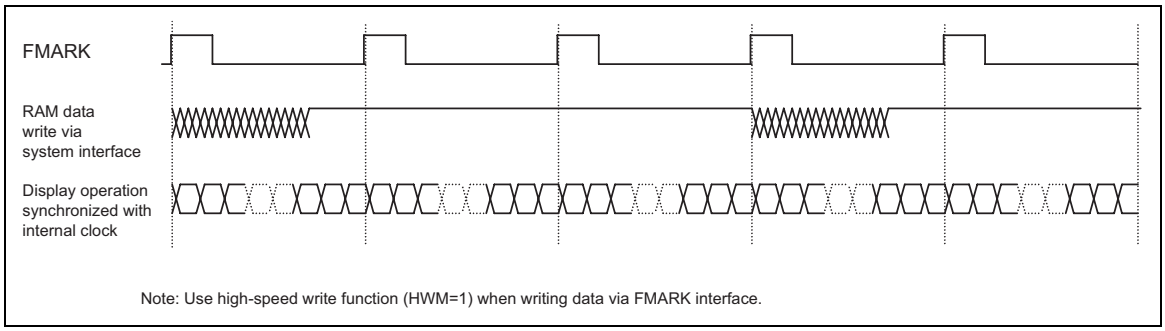


Figure 54 Moving Picture Data Transfers via FMARK Function

When transferring data in synchronization with FMARK signal, minimum RAM data write speed and internal clock frequency must be taken into consideration. They must be more than the values calculated from the following equations.

Internal clock frequency (fosc) [Hz]

$$= FrameFrequency \times (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) \times 16(clocks) \times \mathrm{var}iance$$

$$RAMWriteSpeed(\min.)[Hz] > \frac{240 \times DisplayLines(NL)}{(FrontPorch(FP) + BackPorch(BP) + DisplayLines(NL) - m\arg ins) \times 16(clocks) \times \frac{1}{fosc}}$$

Note: When RAM write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM data write speed and internal clock frequency is as follows.

[Example]

Panel size	240 RGB × 320 lines (NL = 6'h13)
Total number of lines (NL)	320 lines
Back/front porch	14/2 lines (BP = 4h'E, FP = 4'h2)
Frame marker position (FMP)	Display end line: 320th (FMP = 9'h14E)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz]
= 60 Hz × (320 + 2 + 14) lines × 16 clocks × 1.1 / 0.9 = 394 kHz

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one FMARK cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz]
> 240 × 320 / {((2+14 + 320 - 2) lines × 16 clocks) × 1/394 kHz} = 5.67 MHz

Notes: 1. In this example, it is assumed that the R61505 starts writing data in the internal RAM on the rising edge of FMARK.
2. There must be at least a margin of 2 lines between the line to which the R61505 has just written data and the line where display operation on the LCD is performed.
3. The FMARK signal output position is set to the line specified by FMP[8:0] bits.

In this example, RAM write operation at a speed of 5.67MHz or more, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the R61505 starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

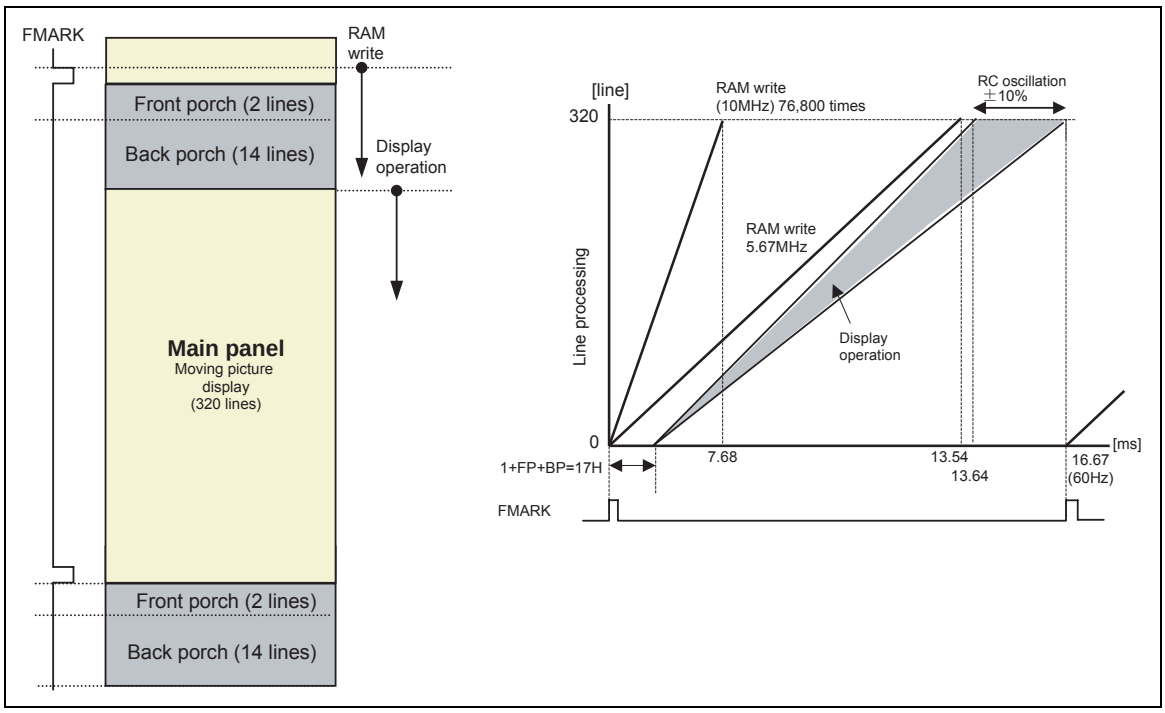


Figure 55 Write/Display Operation Timing

Notes on Display Operation Synchronous Data Transfer Using FMARK Signal

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margin in setting RAM write speed for this operation.

2. Use high-speed write function (HWM = 1).

High-Speed RAM Write Function

The R61505 supports high-speed RAM write function to write data to each line of window address area at a time. This function makes the R61505 available with the applications, which require high-speed, low-power-consumption data write operation such as color moving picture display.

When enabling high-speed RAM write function (HWM = "1"), the data is first stored in the internal register of the R61505 in order to rewrite the RAM data in each horizontal line of the window address area at a time. Also, when transferring the data from the internal register to the internal RAM, the data written in the next line of the window address area can be transferred to the internal register of the R61505. The high-speed write function minimizes the number of RAM access in write operation and enables high-speed consecutive RAM write operation required for moving picture display with low power consumption.

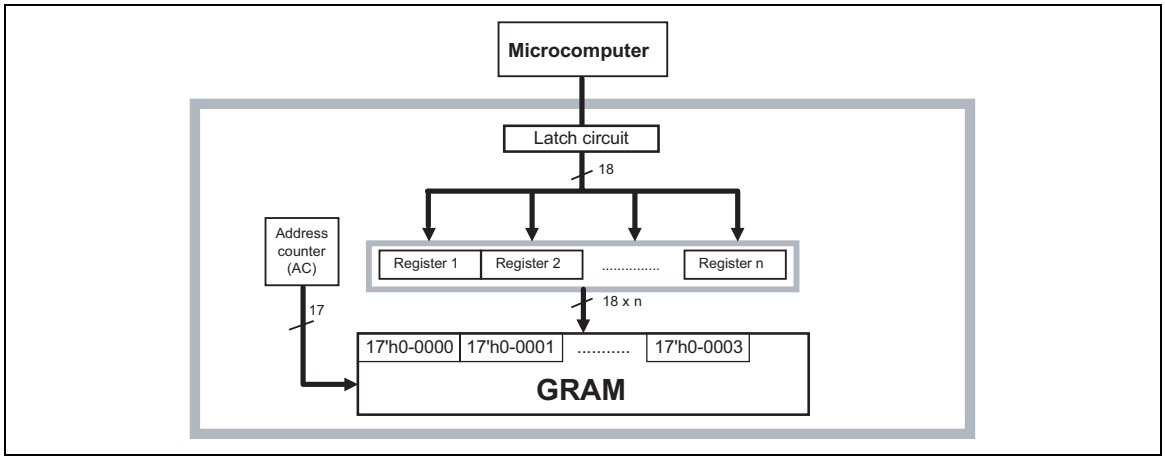


Figure 56 High-Speed Consecutive RAM Write Operation

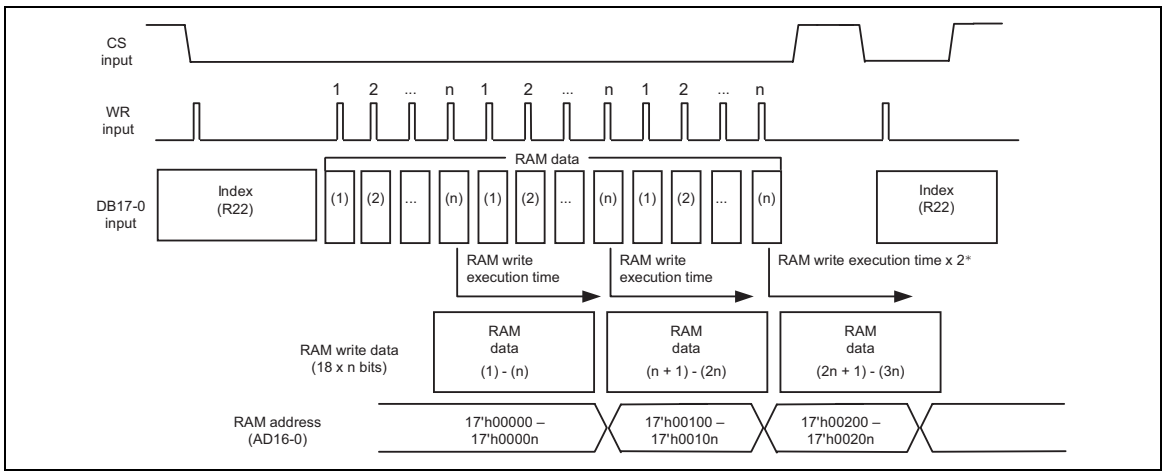


Figure 57 Example of High-Speed RAM Write Operation (HWM = 1)

Note: When switching from high-speed RAM write operation to index write operation, wait at least for two normal RAM write bus cycle periods (2 x t_{cycw}) before executing a next instruction.

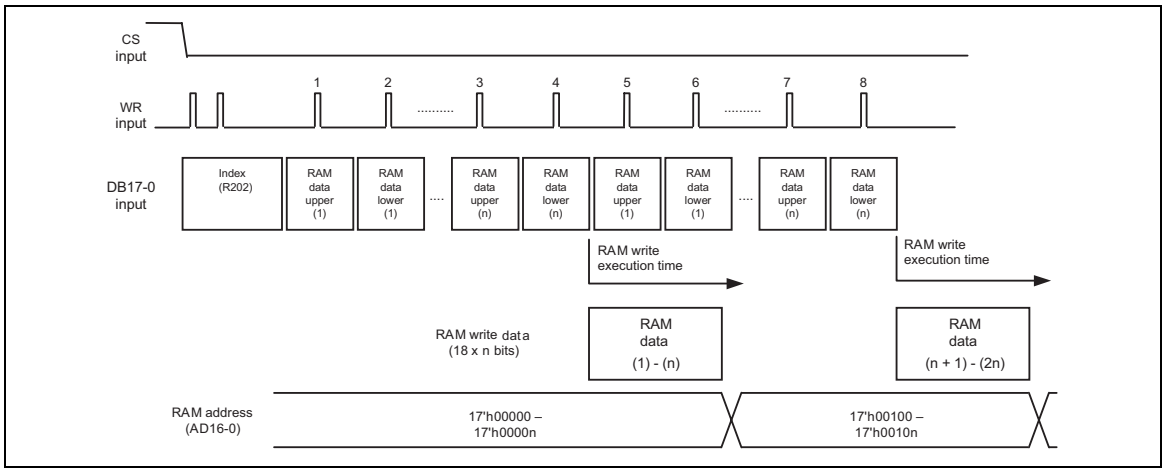


Figure 58 Example of High-Speed RAM Write Operation via 9-Bit Interface

Note: In high-speed RAM write operation, the R61505 writes data in units of n words. When using 9-bit interface, the R61505 performs write operation 2 x n times in the internal register before writing the data in each line of the window address area.

Notes on High-Speed RAM Write Function

1. In high-speed RAM write mode, the R61505 performs write operation to the internal RAM in units of lines. If the data inputted to the internal write register is not enough to rewrite the data in the horizontal line of the window address area, the data is not written correctly in that line address.

2. If the IR is set to 22h when HWM = "1", the R61505 always performs RAM write operation. With this setting, the R61505 does not perform RAM read operation. Make sure to set HWM = 0, when performing RAM read operation.

3. The high-speed RAM write function cannot be used when writing data in normal RAM write function mode. When switching form one write mode to the other, change modes first and set AD16-0 (RAM address set) before starting write operation.

Table 69 RAM Write Operation

	Normal RAM Write (HWM = 0)	High-Speed RAM Write (HWM = 1)
BGR function	Available	Available
RAM address set	In units of words	In units of words
RAM read	In units of words	Not available
RAM write	In units of words	In units of words
Window address	In units of words (minimum window address area: 1 word x 1 line)	In units of words (minimum window address area: 8 words x 1 line)
External display interface	Available	Available
AM	AM = 1/0	AM = 0

High-Speed RAM Data Write in a Window Address Area

The R61505 can perform consecutive high-speed data rewrite operation within a rectangular area (minimum: 8 words x 1 line) made in the internal RAM with the following settings.

When writing data to the internal RAM using high-speed RAM write function, make sure each line of the window address area is overwritten at a time. If the data buffered in the internal register of the R61505 is not enough to overwrite the horizontal line in the window address area, the data is not written correctly in that line.

The following is an example of writing data in the window address area using high-speed write function when a window address area is made by setting HSA = 8'h12, HEA = 8'hA7, VSA = 9'h020, and VEA = 9'h05B.

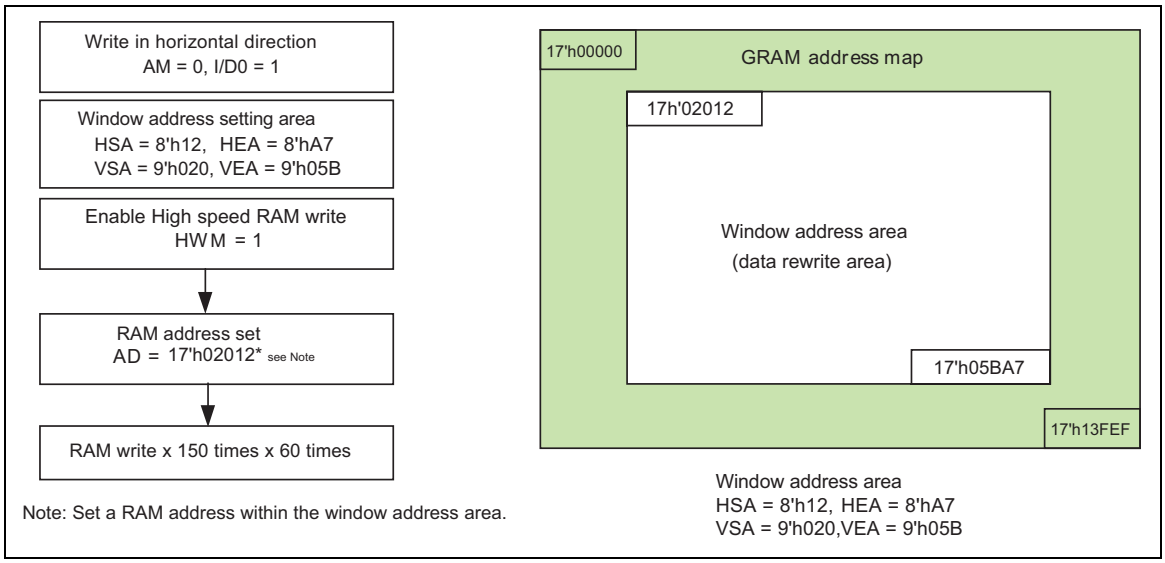


Figure 59 High-Speed RAM Write Operation in the Window Address Area

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the R61505 to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area setting range]
(Horizontal direction) 8'h00 ≤ HSA ≤ HEA ≤ 8'hEF
(Vertical direction) 9'h000 ≤ VSA ≤ VEA ≤ 9'h13F

[RAM Address setting range]
(RAM address) HSA ≤ AD7-0 ≤ HEA
VSA ≤ AD16-8 ≤ VEA

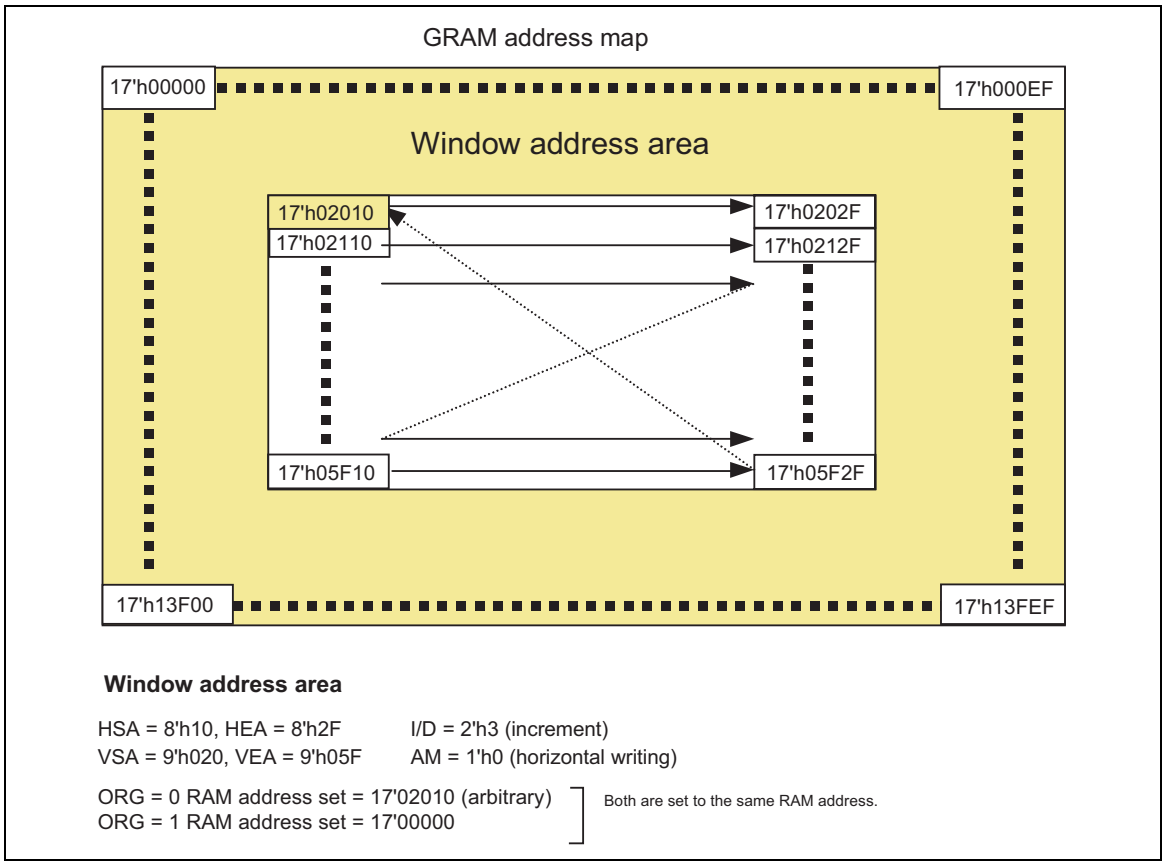
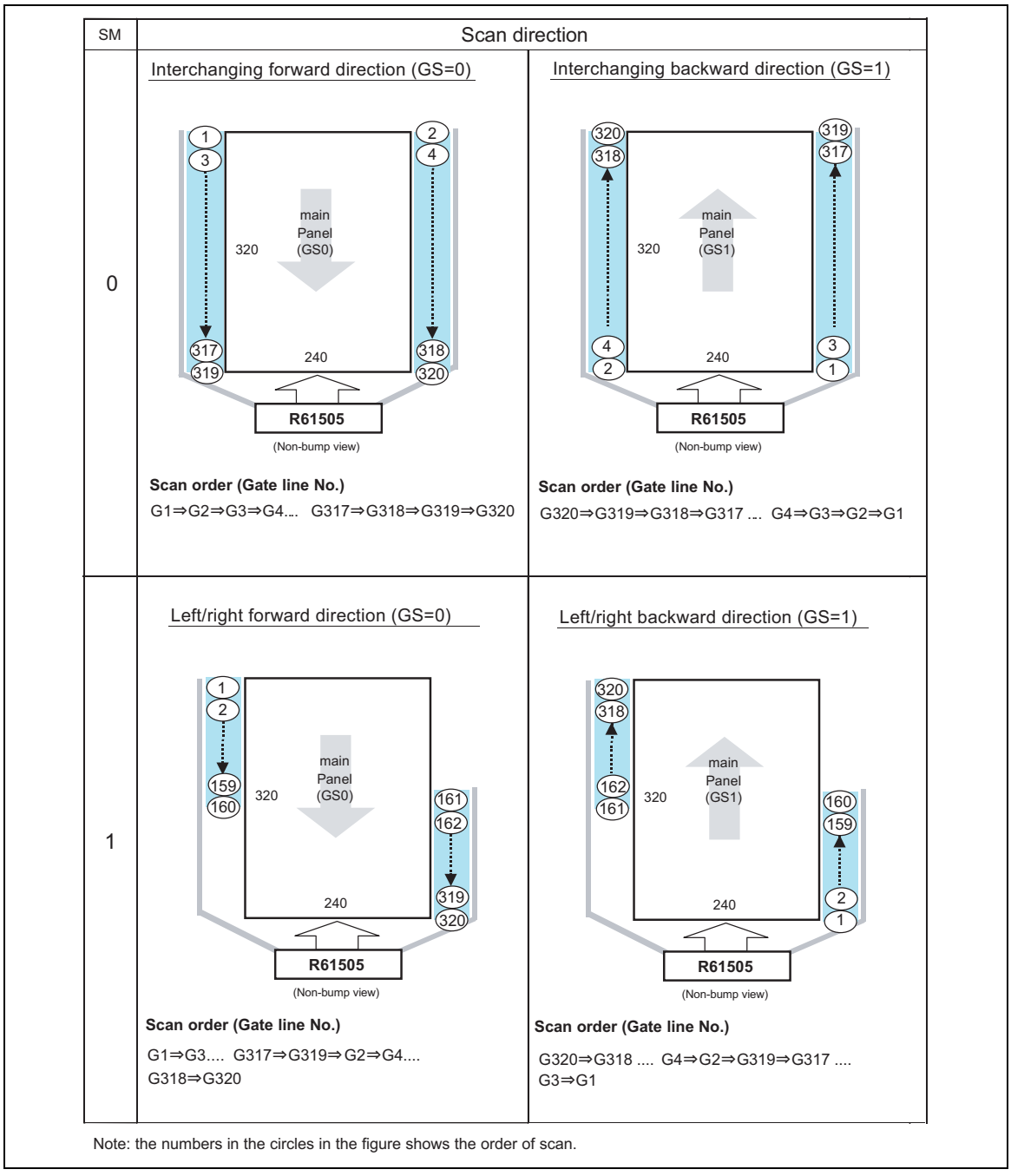


Figure 60 Automatic Address Update within a Window Address Area

Scan Mode Setting

The R61505 can set the gate pin assignment and the scan direction in the following 4 different ways by setting SM and GS bits to realize various connections between the R61505 and the LCD panel.



Note: the numbers in the circles in the figure shows the order of scan.

Figure 61

8-Color Display Mode

The R61505 has a function to display in eight colors. In this display mode, only V0 and V31 are used and power supplies to other grayscales (V1 to V30) are turned off to reduce power consumption.

In 8-color display mode, the γ-adjustment registers P0KP0-P0KP5, P0KN0-P0KN5, P0RP0, P0RP1, P0RN0, P0RN1, P0FP0-P0FP3, and P0FN0-P0FN3, are disabled and the power supplies to V1 to V30 are halted. The R61505 does not require GRAM data rewrite for 8-color display by writing the MSB to the rest in each dot data to display in 8 colors.

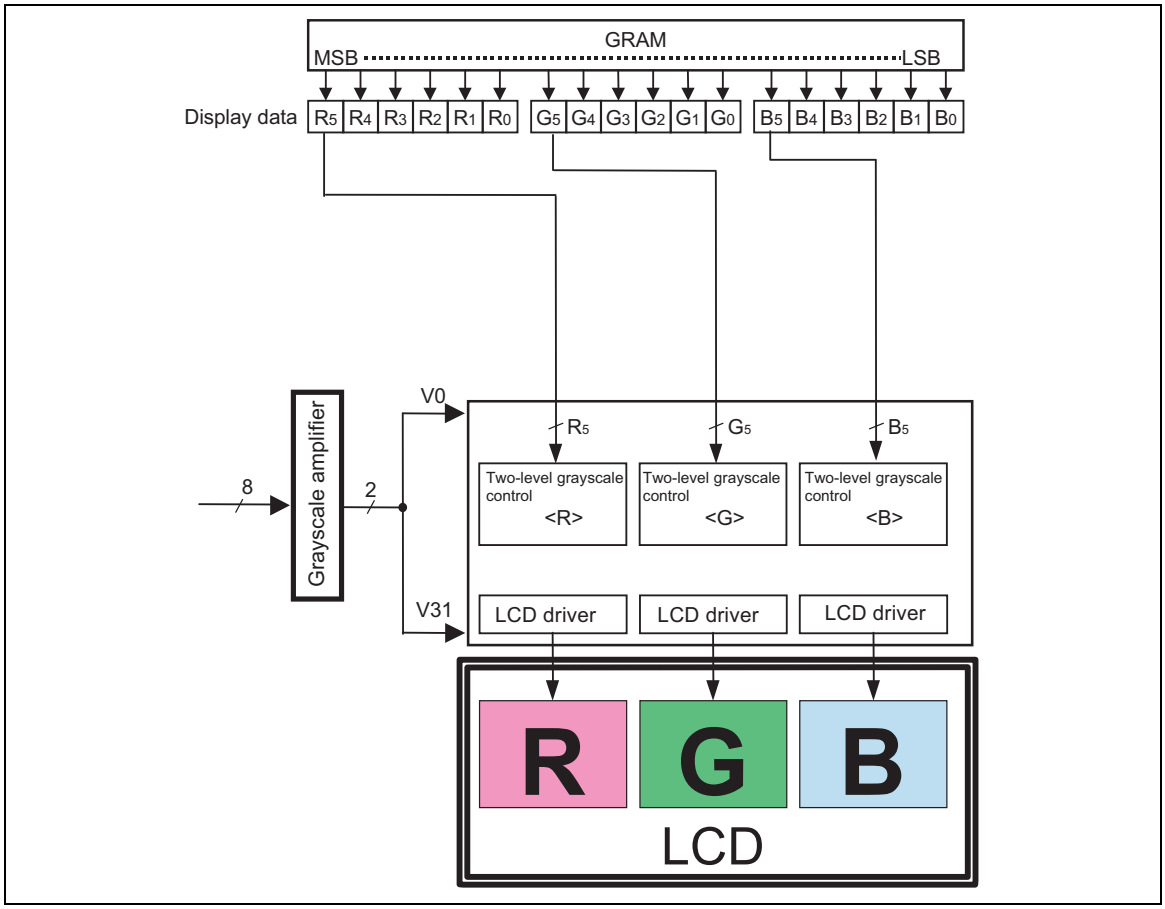


Figure 62 8-Color Display Mode

Line Inversion AC Drive

The R61505, in addition to frame-inversion liquid crystal alternating current drive, supports one-line inversion alternating current drive.

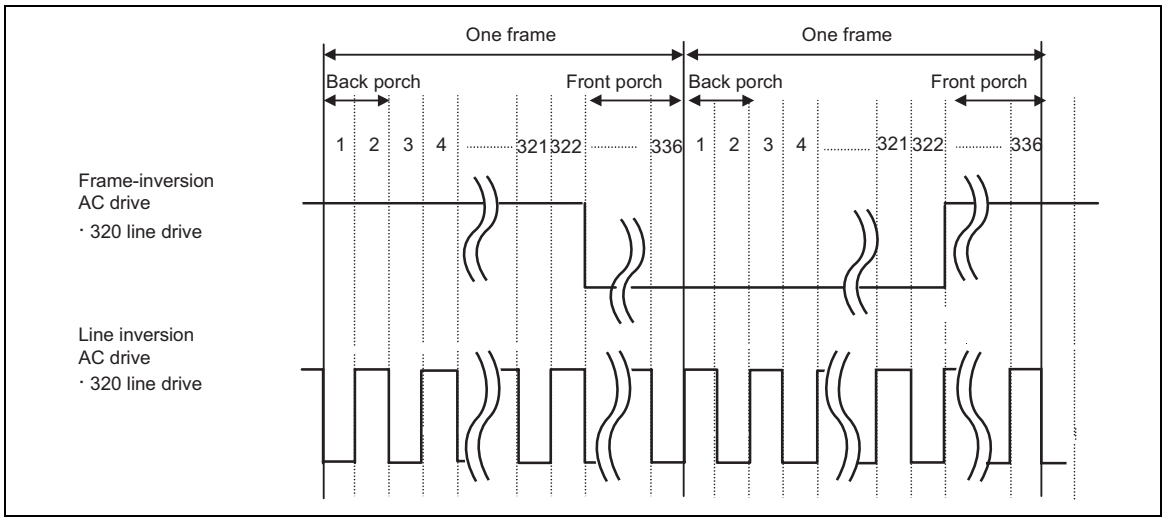


Figure 63 Example of Alternating Signals for n-Line Inversion

Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different LCD driving methods. In case of frame-inversion AC drive, the polarity is inverted as the R61505 draws one frame, which is followed by a blank period lasting for (BP+FP) periods. In case of line inversion AC drive, polarity is inverted as the R61505 draws one line, and a blank period lasting for (BP+FP) periods is inserted when the R61505 draws one frame.

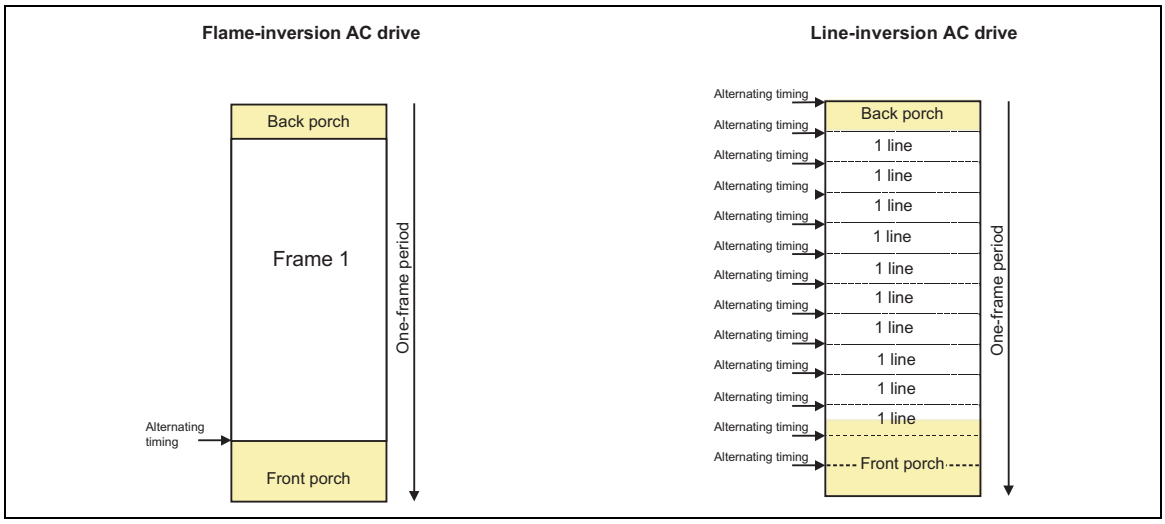


Figure 64 Alternating Timing

Note: Frame inversion AC drive is available only in 8-color display mode. Check the quality of display on the panel.

Frame-Frequency Adjustment Function

The R61505 supports a function to adjust frame frequency. The frame frequency for driving liquid crystal can be adjusted by setting the DIV, RTN bits without changing the oscillation frequency.

The R61505 allows changing the frame frequency depending on whether moving picture or still picture is displayed on the screen. In this case, set a high oscillation frequency. By changing the DIV and RTN settings, the R61505 can operate at high frame frequency when displaying a moving picture, which requires the R61505 to rewrite data in high speed, and it can operate at low frame frequency when displaying a still picture.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The following equation represent the relationship between liquid crystal drive duty and frame frequency. The frame frequency can be changed by setting the 1H period adjustment bit (RTN) and the operation clock frequency division ratio setting bit (DIV).

Equation for calculating frame frequency

$$FrameFrequency = \frac{fosc}{NumberofClocks/line \times DivisionRatio \times (Line + FP + BP)}[Hz]$$

fosc: RC oscillation frequency
Number of clocks per line: RTN bit
Division ratio: DIV bit
Line: number of lines to drive the LCD panel (NL bit)
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when Maximum Frame Frequency = 60 Hz

Number of lines: 320 lines
1H period: 16 clock cycles (RTNI/E[4:0] = “10000”)
Division ratio of operating clock: 1/1
Front porch: 2 lines
Back porch: 14 lines

$$fosc = 60\ (Hz) \times 16\ (clocks) \times 1/1 \times (320+2+14)\ (lines) = 323\ (kHz)$$

In this case, the RC oscillation frequency must be set to 323kHz. Adjust the value of external resistor connected to the RC oscillator so that RC oscillation frequency becomes 323kHz.

Partial Display Function

The partial display function allows the R61505 to drive lines selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven at non-lit display level to reduce power consumption.

The power efficiency can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

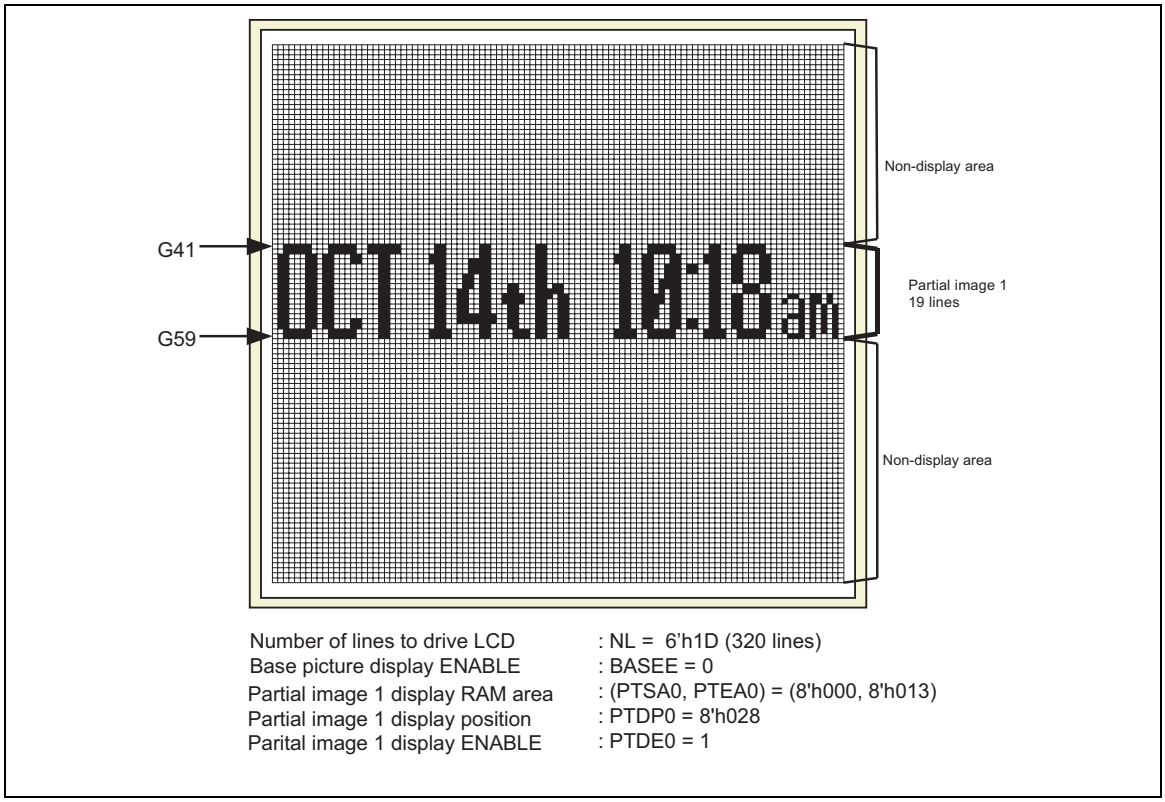


Figure 65 Partial Display

Note: See the "RAM Address and Display Position on the Panel" (p.114) for details on the relationship between the display positions of partial images and respective RAM area setting.

Liquid Crystal Panel Interface Timing

The relationships between RGB interface signals and liquid crystal panel control signals in internal operation and RGB interface operations are as follows

Internal Clock Operation

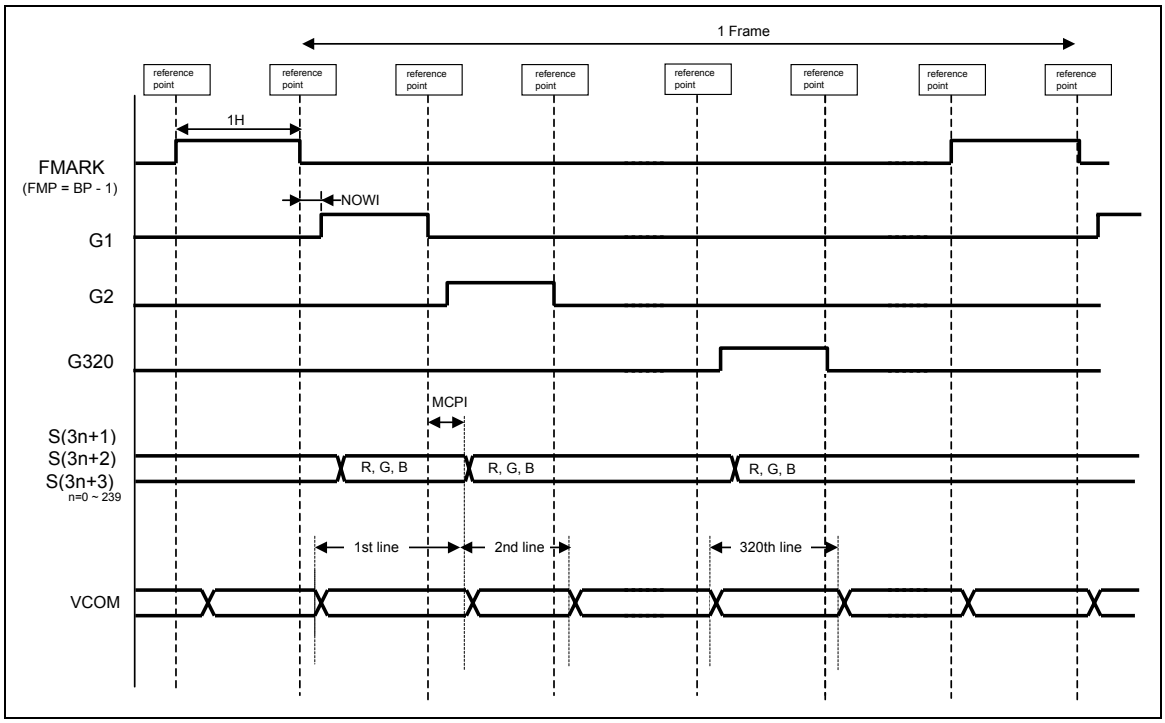


Figure 66

RGB Interface Operation

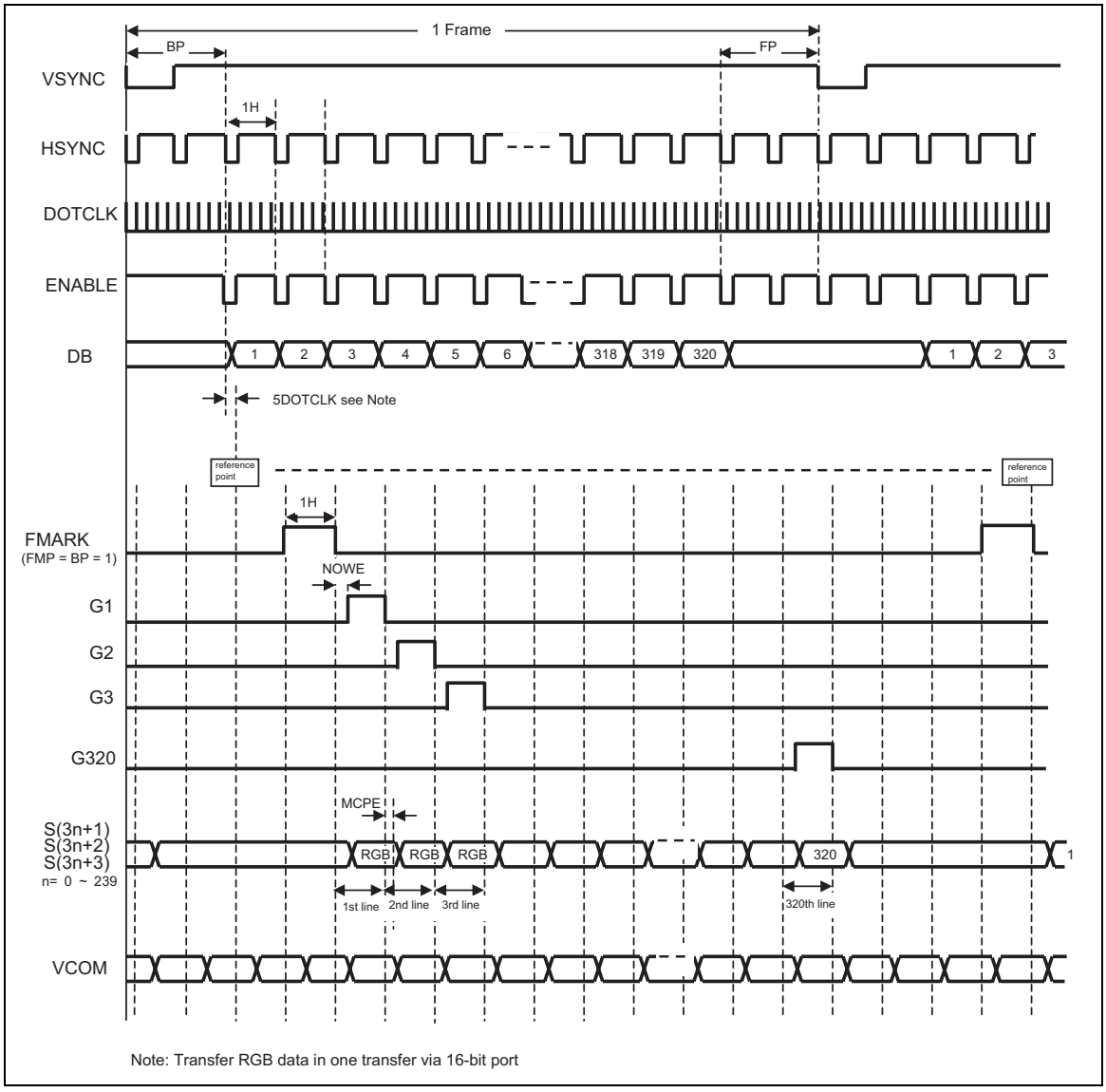


Figure 67

Oscillator

The R61505 generates RC oscillation with the internal RC oscillator to which an external oscillation resistor is connected between the OSC1 and OSC2 pins. The oscillation frequency varies depending on the value of external resistor, wiring length, operating power supply voltage. For example, the oscillation frequency becomes lower by connecting an external resistor of a larger resistance, or lowering supply voltage.

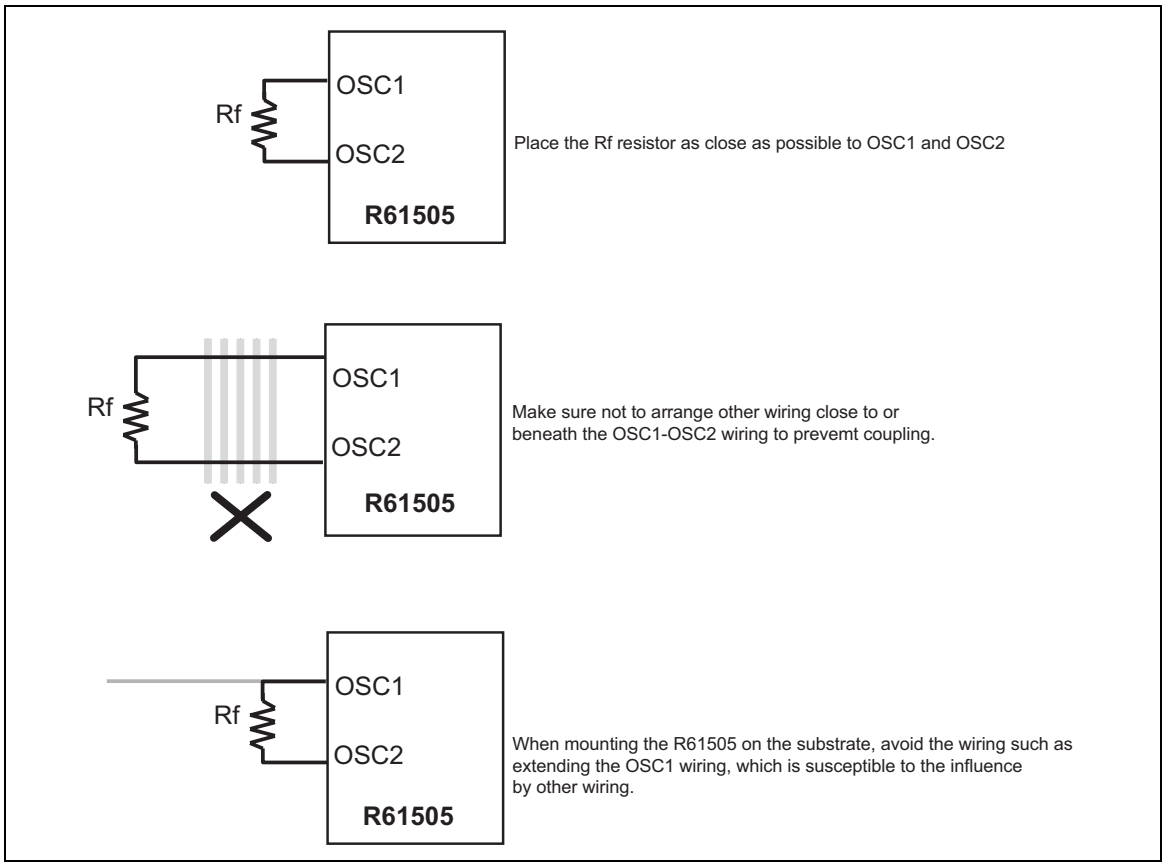


Figure 68

γ Correction Function

The R61505 supports γ-correction function to display in 262,144 colors simultaneously using gradient-adjustment, amplitude-adjustment, fine-adjustment, tap-adjustment, and voltage division ratio adjustment registers. Each register consists of positive-polarity register and negative-polarity register to allow optimal gamma correction setting for the characteristics of the panel by enabling different settings for positive and negative polarities.

γ Correction Registers

The γ-correction registers of the R61505 consists of gradient-adjustment, amplitude-adjustment, fine-adjustment, tap-adjustment, and voltage division ratio adjustment registers to correct grayscale voltage levels according to the gamma characteristics of the liquid crystal panel. These register settings make adjustments to the relationship between grayscale number and grayscale voltage and the setting can be made differently for positive and negative polarities (the reference level and the register settings are the same for all RGB dots). The function of each register is as follows.

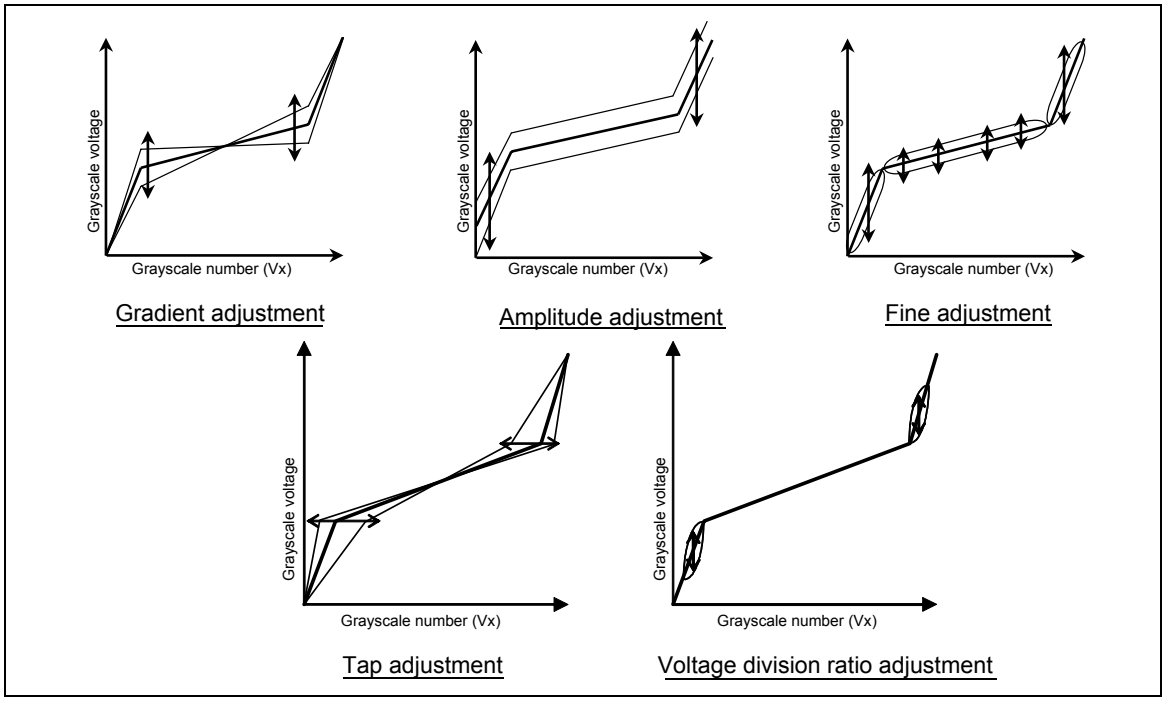


Figure 69

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient, which represents the relationship between grayscale and voltage, without changing the dynamic range. The grayscale voltages for middle grayscale number can be adjusted by this register setting.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage.

3. Fine adjustment registers

The fine adjustment registers are used for minute adjustment of grayscale voltage levels.

4. Tap adjustment registers

The tap adjustment registers are for selecting two tap voltage supply points from V3 to V6 and from V25 to V28 by using selector.

5. Voltage division ratio adjustment registers

The voltage division ratio adjustment registers are used to change the division ratios between V0 and V1 and between V30 and V31.

Table 70 γ correction Registers

Register	Positive	Negative	Function
Gradient	P0RP0 [2:0]	P0RN1 [2:0]	Grayscale V4 variable resistance
	P0RP1 [2:0]	P0RN0 [2:0]	Grayscale V27 variable resistance
Amplitude	V0RP0 [4:0]	V0RN1 [4:0]	Voltage level for grayscale V0
	V0RP1 [4:0]	V0RN0 [4:0]	Voltage level for grayscale V31
Fine adjustment	P0KP0 [2:0]	P0KN5 [2:0]	Voltage level for grayscale V1
	P0KP1 [2:0]	P0KN4 [2:0]	Voltage level for grayscales V3, V4, V5, V6
	P0KP2 [2:0]	P0KN3 [2:0]	Voltage level for grayscale V10
	P0KP3 [2:0]	P0KN2 [2:0]	Voltage level for grayscale V21
	P0KP4 [2:0]	P0KN1 [2:0]	Voltage level for grayscales V28, V27, V26, V25
	P0KP5 [2:0]	P0KN0 [2:0]	Voltage level for grayscales V30
	P0FP0 [1:0]	P0FN3 [1:0]	Division ratio between V0 and V1
	P0FP1 [1:0]	P0FN2 [1:0]	P0FP1[1:0]: specify either one of grayscales V3, V4, V5, V6 for the P0KP1[2:0] level P0FN2[1:0]: specify either one of grayscales V3, V4, V5, V6 for the P0KN4[2:0] level
	P0FP2 [1:0]	P0FN1 [1:0]	P0FP2[1:0]: specify either one of grayscales V28, V27, V26, V25 for the P0KP4[2:0] level P0FN1[1:0]: specify either one of grayscales V28, V27, V26, V25 for the P0KN1[2:0] level
	P0FP3 [1:0]	P0FN0 [1:0]	Division ratio between V30 and V31

γ Correction Register Settings and γ Curve Relationship

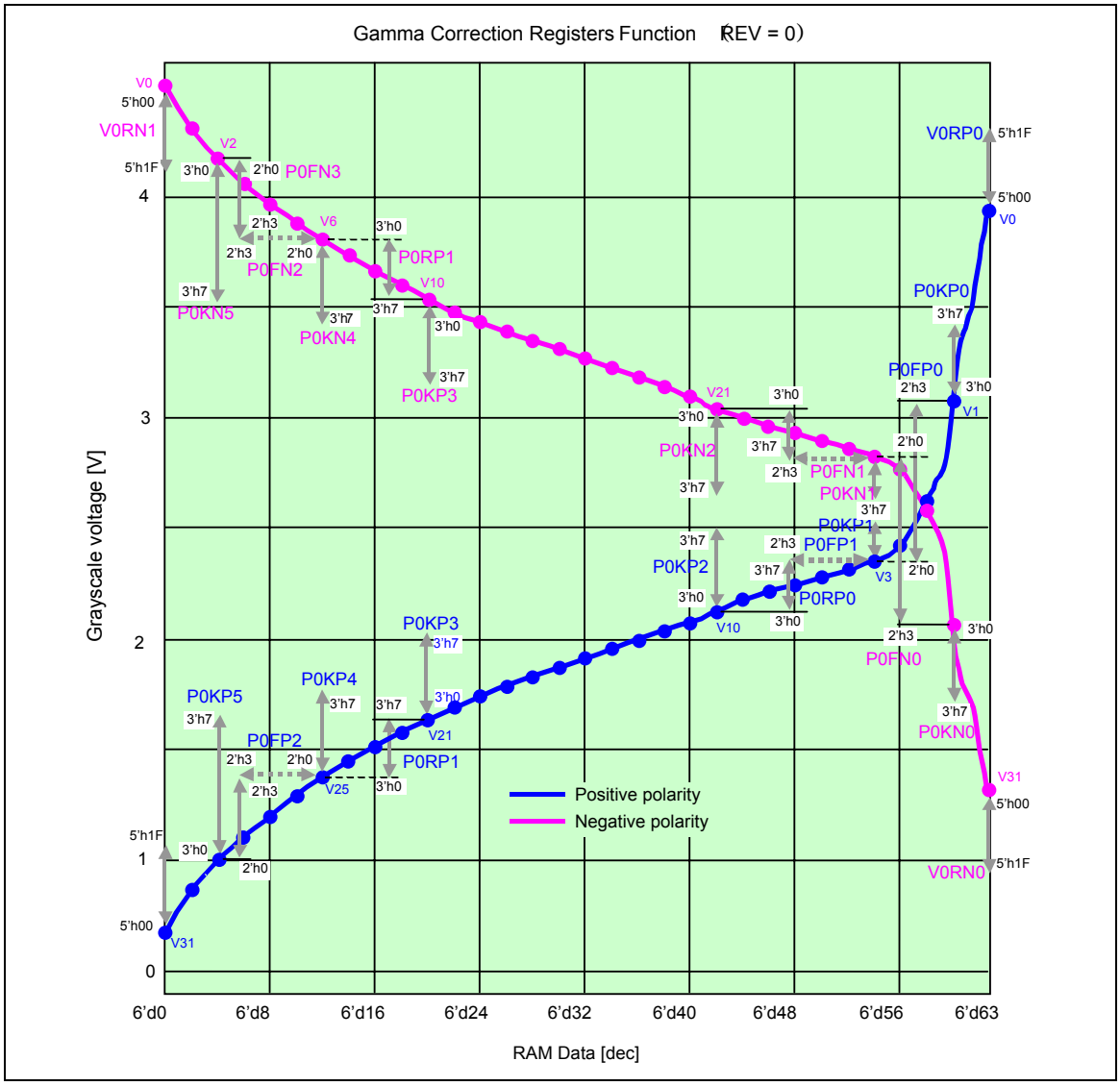


Figure 70

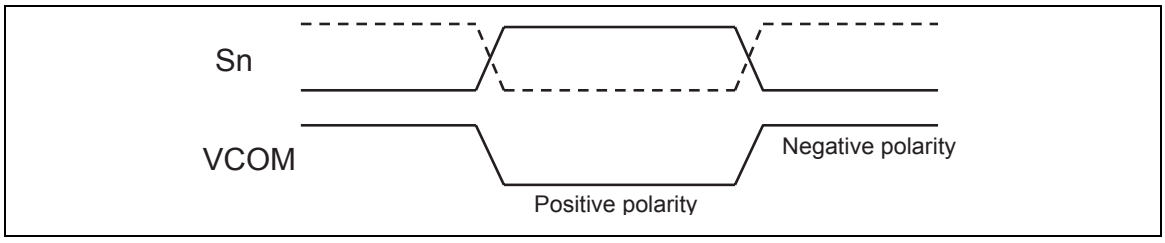


Figure 71 Source Output Waveform and Vcom Polarity Relationship

Power-Supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the R61505.

Power Supply Circuit Connection Example 1 (Vci1 = VciOUT)

In the following example, the VciOUT level is adjusted internally in the VciOUT output circuit.

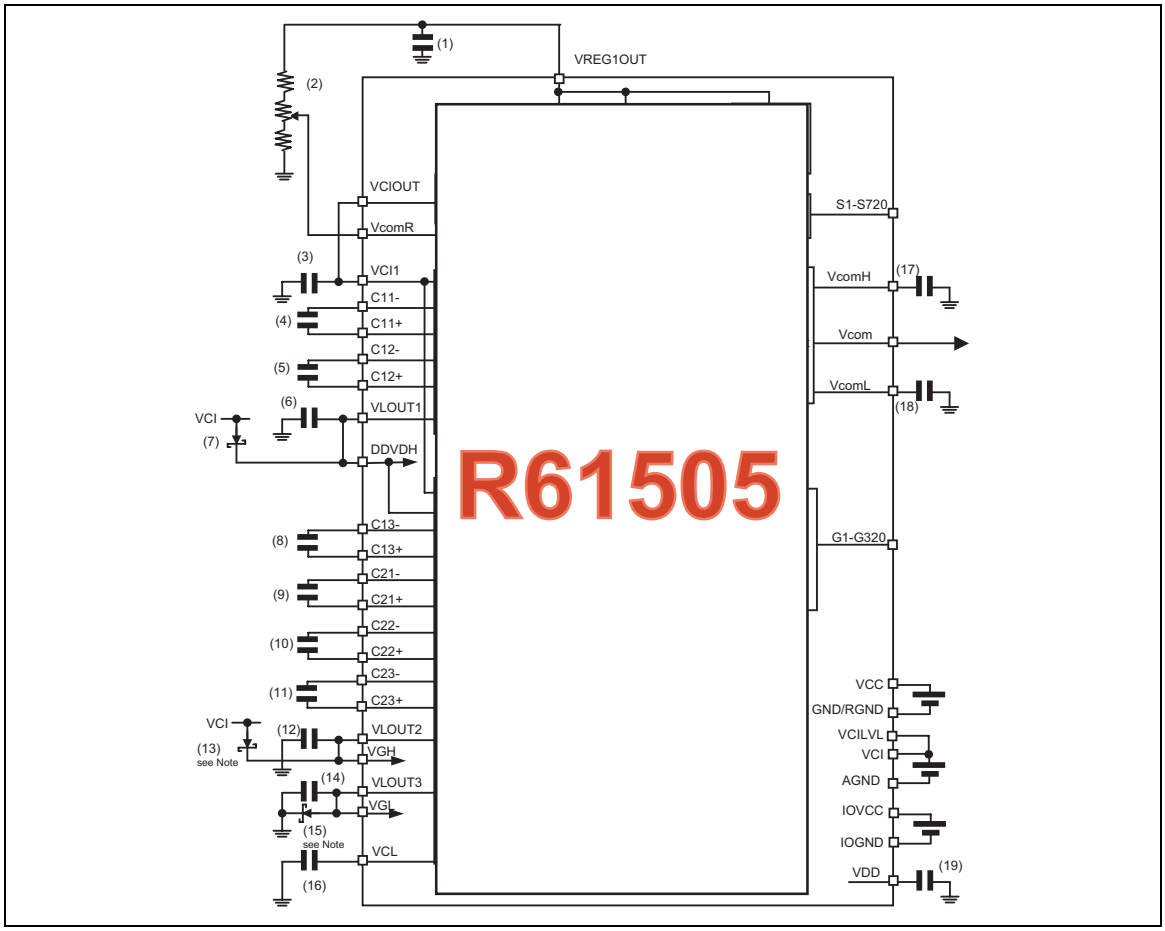


Figure 72

Note: The wiring resistances between the schottky diode and GND/VGL must be 10Ω or less.

Power Supply Circuit Connection Example 2 (Vci1 = Vci Direct Input)

In the following example, the electrical potential Vci is directly applied to Vci1. In this case, the VciOUT level cannot be adjusted internally but step-up operation becomes more effective.

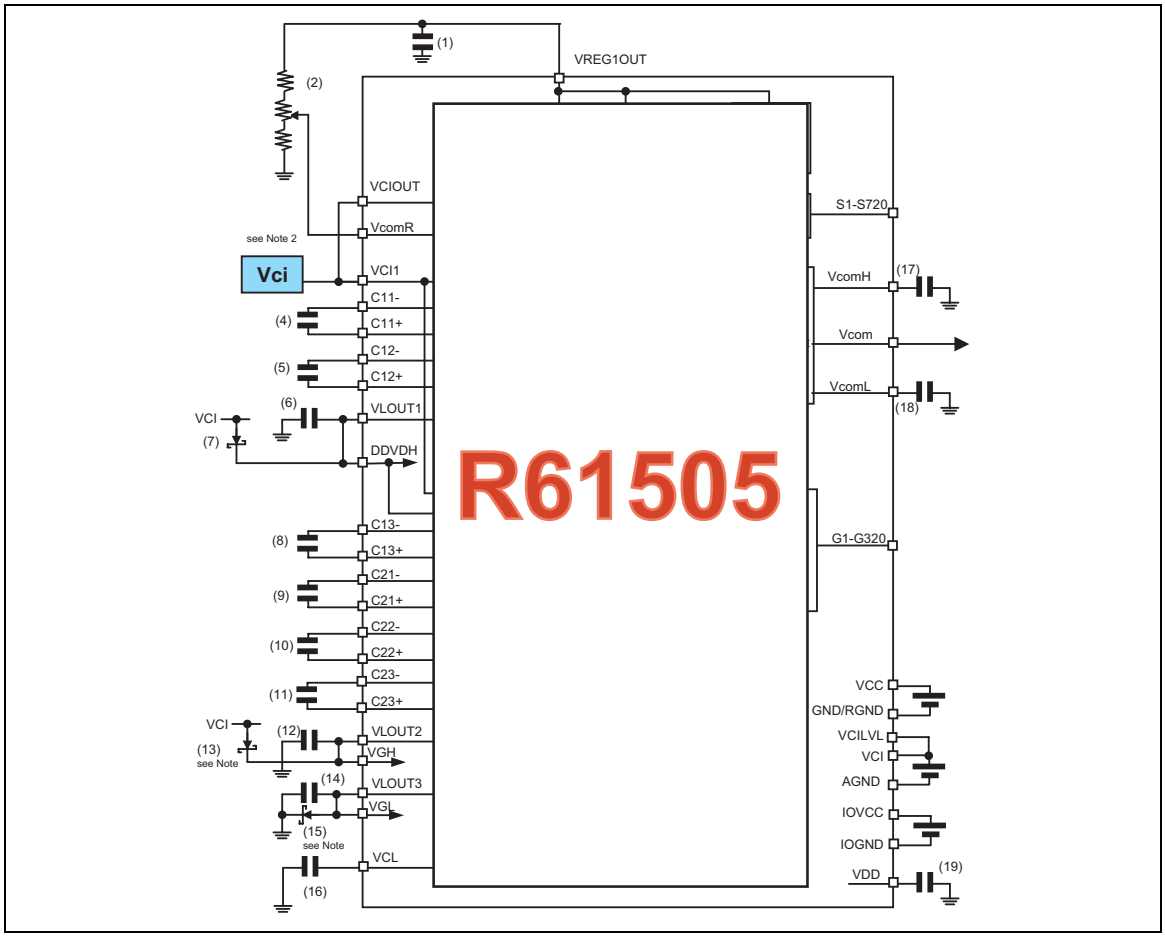


Figure 73

Notes: 1. The wiring resistances between the schottky diode and GND/VGL must be 10Ω or less.
2. When directly applying the Vci level to Vci1, set VC = 3'h7. Capacitor connection to VciOUT is not necessary.

Specifications of Power-supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the R61505 are as follows.

Table 71 Capacitor

Capacitance	Voltage Proof	Pin Connection
1µF (B characteristics)	6 V	(1) VREG1OUT, (3) VciOUT, (4) C11-/+, (5) C12-/+, (8) C13-/+, (16) VCL, (17) VcomH, (18) VcomL, (19) VDD
	10 V	(6) VLOUT1, (9) C21-/+, (10) C22-/+, (11) C23-/+
	25 V	(11) VLOUT2, (13) VLOUT3

Notes: 1. Check with the LC module.
2. The numbers in the parentheses corresponds to the numbers of the elements in Figure 72, Figure 73.

Table 72 Schottky Diode

Specification	Pin Connection
VF < 0.4 V/20 mA@25 °C, VR ≥ 25 V (Recommended diode: HSC226)	(15) GND–VGL, (13) Vci–VGH, (7) Vci–DDVDH

Table 73 Variable Resistor

Specification	Pin Connection
> 200 kΩ	(2) VcomR

Table 74 Internal Logic Power Supply

Capacitance	Voltage Proof (Recommended)	Pin Connection
1µF (B characteristics)	3V	VDD

Table 75 Internal oscillator

Resistance	Usage Condition	Pin Connection
Rf	1mw or less, ±1% or less	OSC1 and OSC2

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61505 and the TFT display application voltage waveforms and electrical potential relationship.

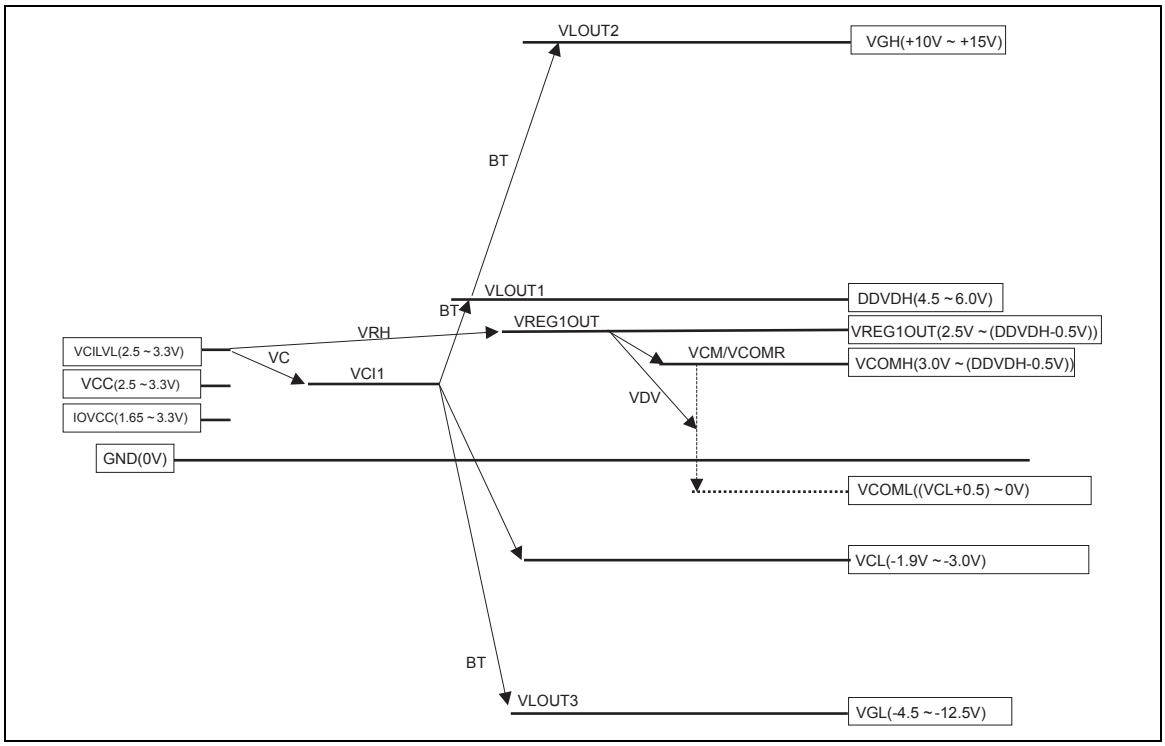


Figure 74

Notes: 1. The DDVDH, VGH, VGL, and VCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at each output level. Make sure that output voltage level in operation maintains the following relationship: (DDVDH – VREG1OUT) > 0.5V, (VcomL – VCL) > 0.5V. Also make sure VGH-VGL ≤ 25V, Vci-VCL ≤ 6V. When the load is on current to the maximum, (DDVDH – VREG1OUT) ≧ 0.3V is also possible. When the alternating cycle of Vcom is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

2. In operation, setting voltages within the respective voltage ranges are recommended.

Liquid Crystal Application Voltage Waveform and Electrical Potential

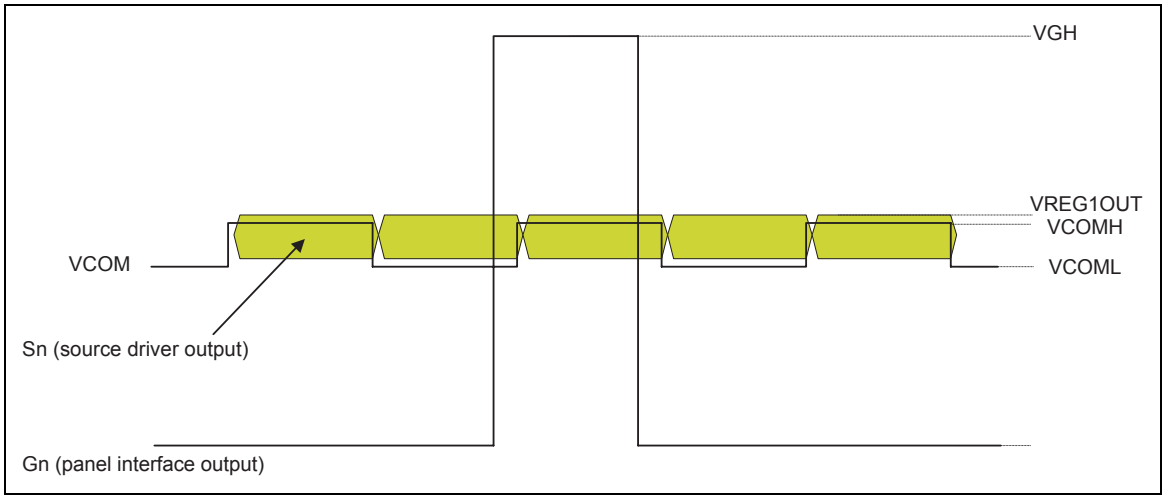


Figure 75

Power Supply Instruction Setting

The following are the sequences for setting power supply ON/OFF instructions. Set power supply ON/OFF instructions according to the following sequences in Display ON/OFF, Sleep set/exit sequences.

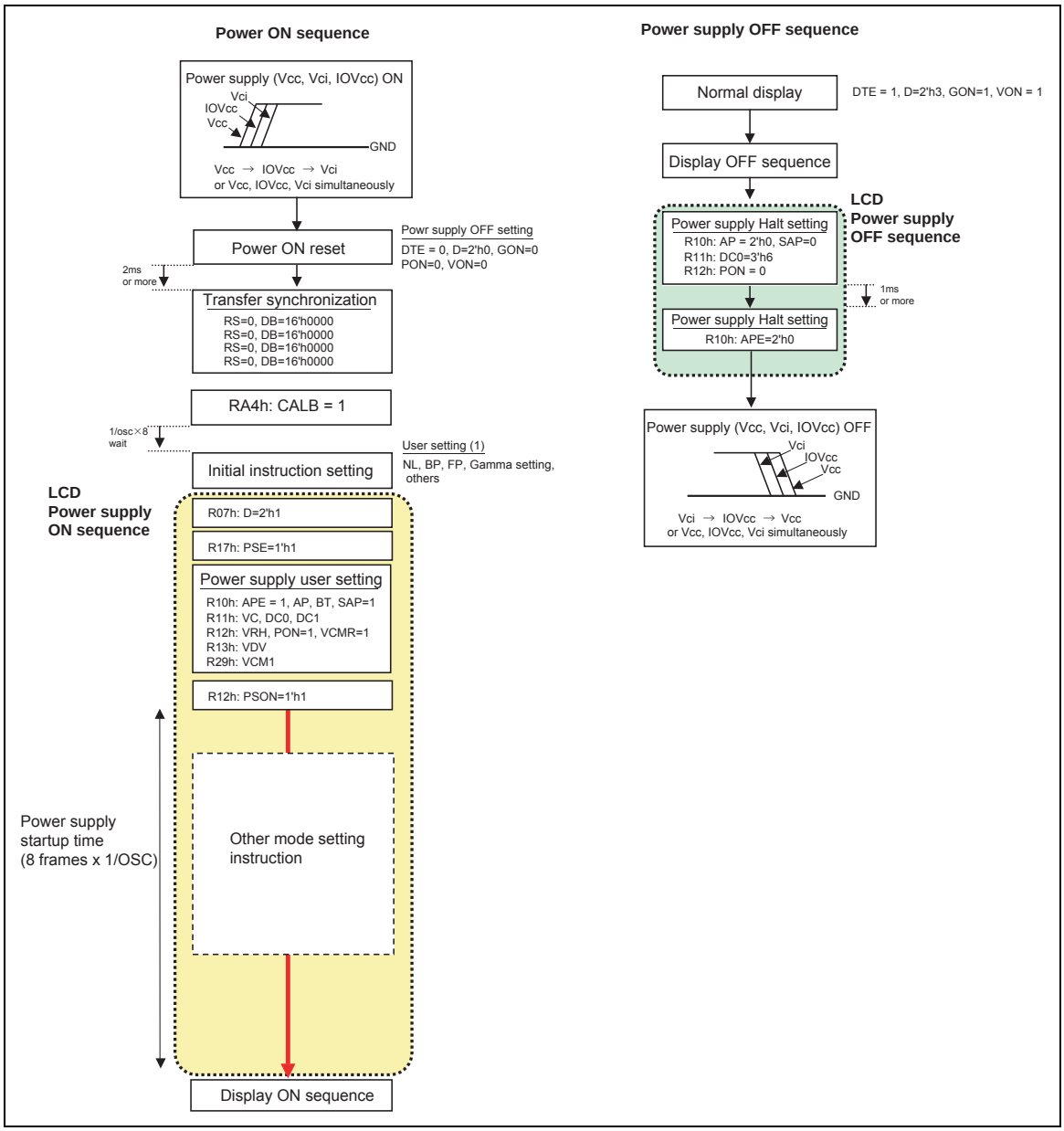


Figure 76

Instruction Setting

The following are the sequences for various instruction settings. When setting instruction in the R61505, follow the relevant sequence below.

Display ON/OFF Sequences

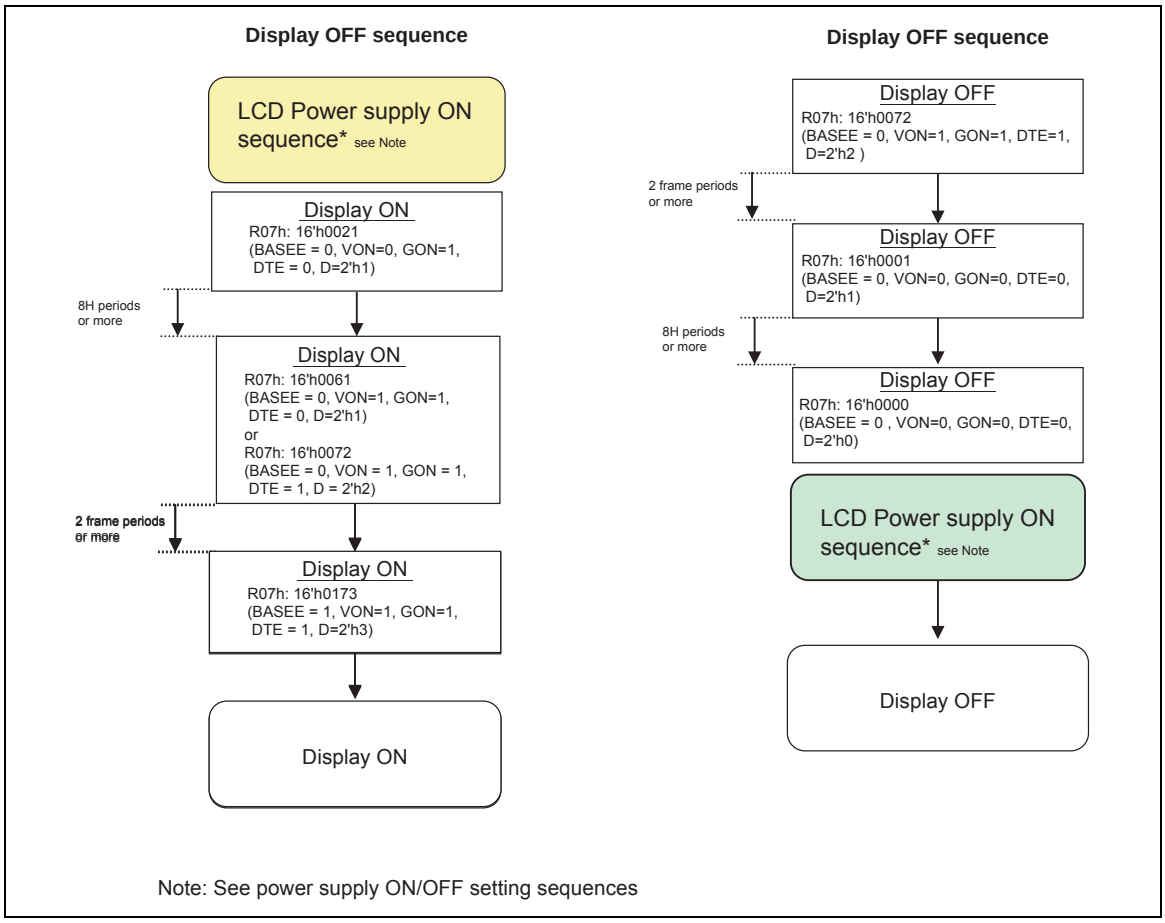


Figure 77

Sleep Mode SET/EXIT Sequences

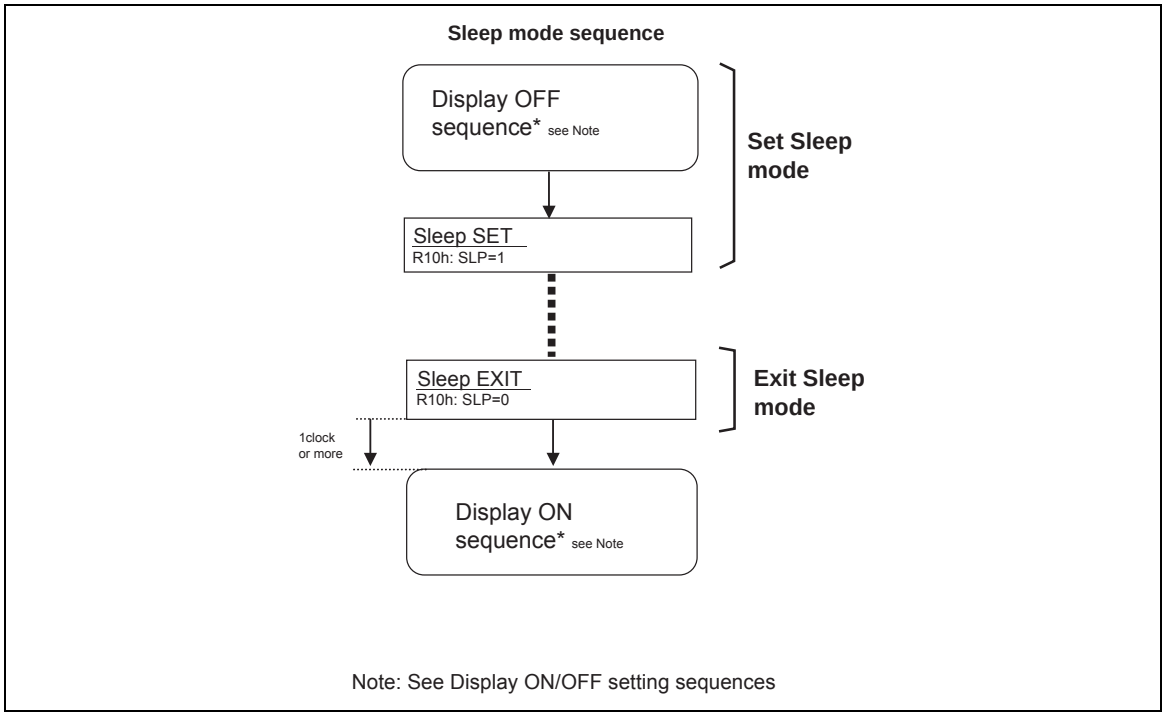


Figure 78

Deep Standby Mode IN/EXIT Sequences

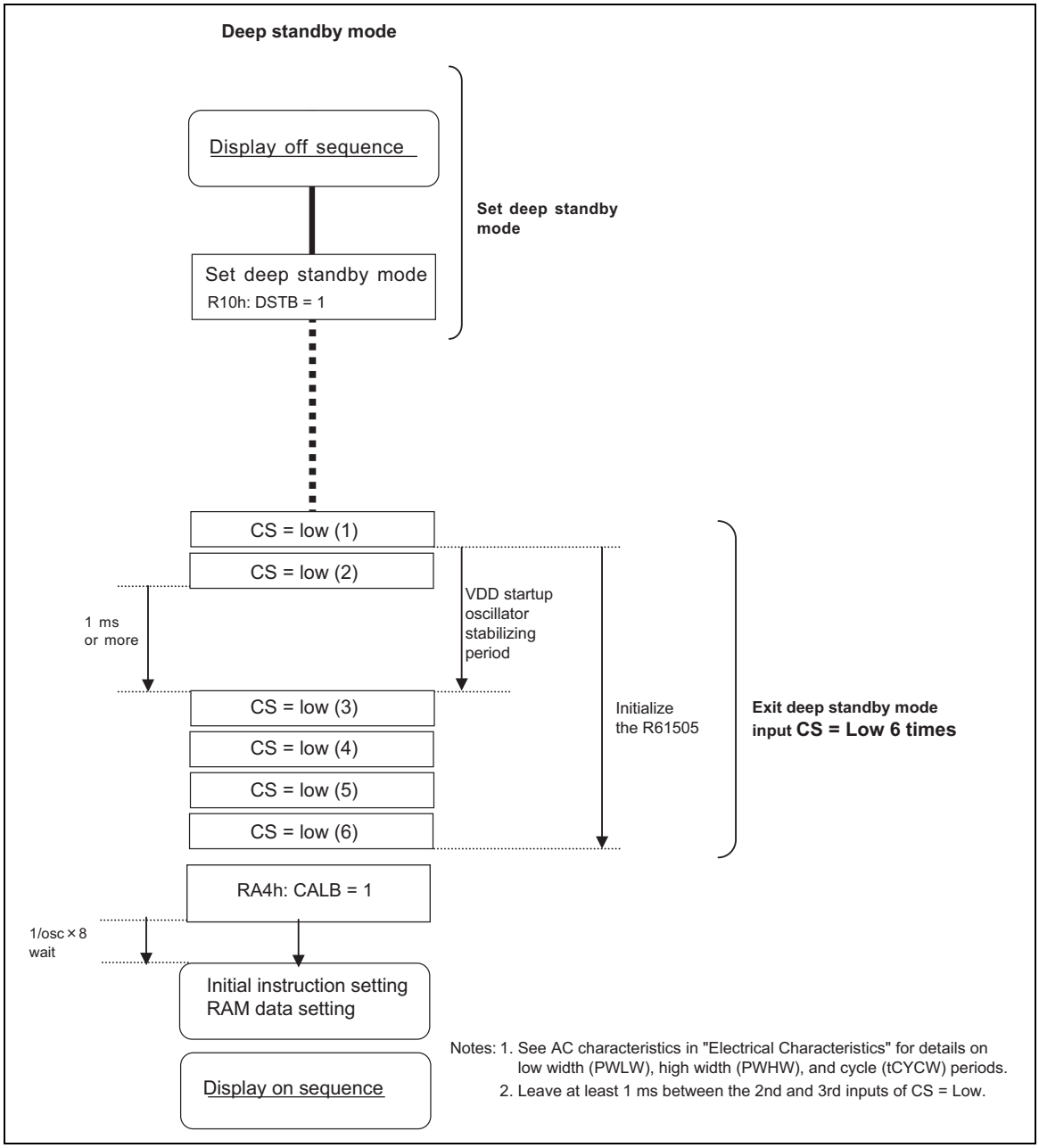


Figure 79

8-Color Mode Setting

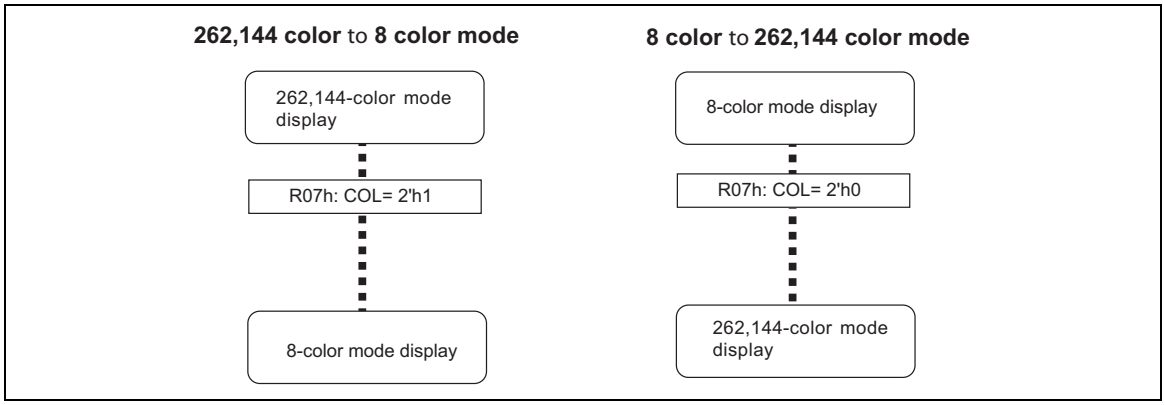


Figure 80]

Partial Display Setting

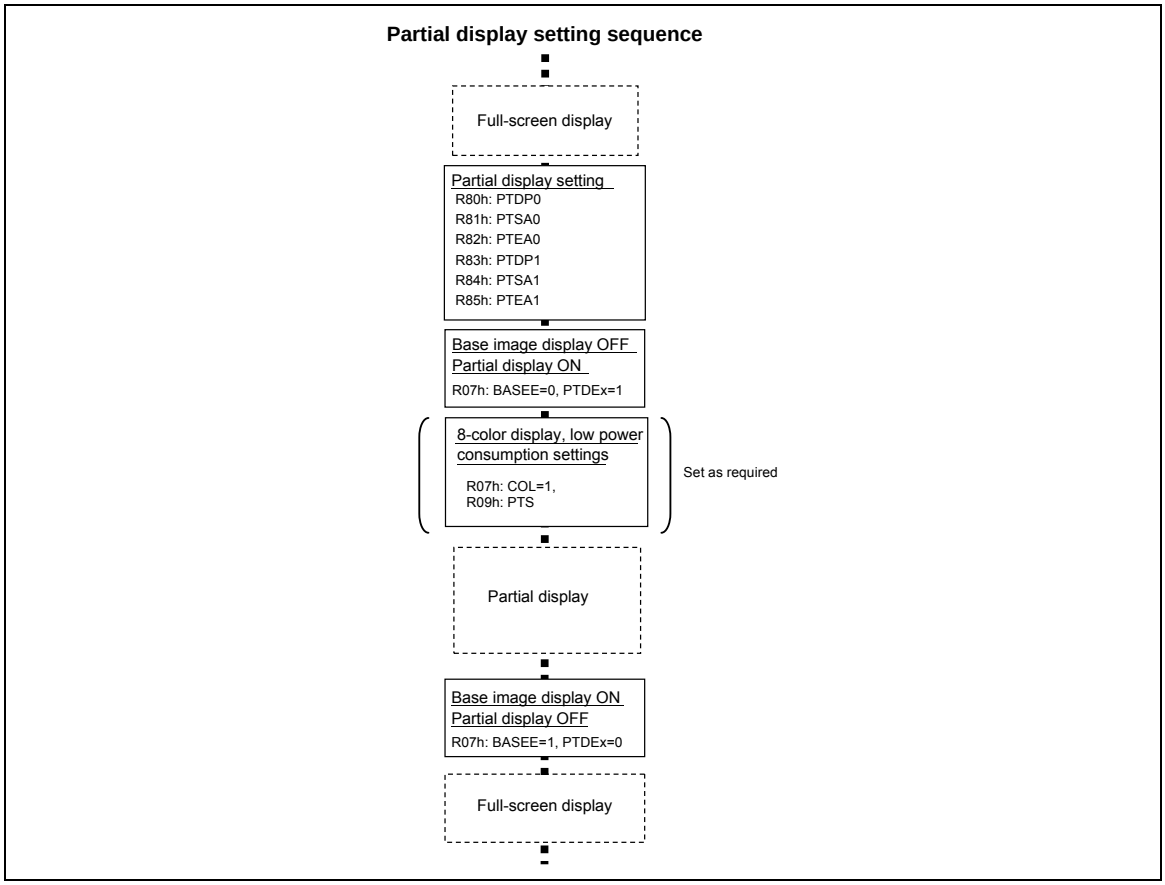


Figure 81

Absolute Maximum Ratings

Table 76 Absolute Maximum Ratings

Item	Symbol	Unit	Ratings	Notes
Power-supply voltage (1)	Vcc, IOVcc	V	-0.3 to +4.6	1, 2
Power-supply voltage (2)	Vci - AGND	V	-0.3 to +4.6	1, 3
Power-supply voltage (3)	DDVDH - AGND	V	-0.3 to +6.5	1, 4
Power-supply voltage (4)	AGND - VCL	V	-0.3 to +4.6	1
Power-supply voltage (5)	DDVDH - VCL	V	-0.3 to +9.0	1, 5
Power-supply voltage (6)	VGH - AGND	V	-0.3 to +16.0	1, 6
Power-supply voltage (7)	AGND - VGL	V	-0.3 to +13.0	1, 7
Input voltage	Vt	V	-0.3 to IOVcc +0.3	1
Operating temperature	Topr	°C	-40 to +85	1, 8
Storage temperature	Tstg	°C	-55 to +110	1

Notes: 1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI within the electrical characteristics conditions in normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.

2. Ensure that Vcc (high) ≥ GND (low) and IOVcc (high) ≥ IOGND (low).
3. Ensure that Vci (high) ≥ AGND (low).
4. Ensure that DDVDH (high) ≥ AGND (low).
5. Ensure that DDVDH (high) ≥ VCL (low).
6. Ensure that VGH (high) ≥ AGND (low).
7. Ensure that AGND (high) ≥ VGL (low).
8. The DC/AC characteristics of die and wafer products are guaranteed at 85 ºC.

Electrical Characteristics

DC Characteristics

Table 77 (Vcc = 2.50V to 3.30V, IOVcc = 1.65V to 3.30V, Ta = –40°C to +85°C[*1])

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
Input high-level voltage (pins other than OSC1)	VIH	V	IOVCC = 1.65 V to 3.30 V	0.80 x IOVcc	-	IOVcc	2, 3
Input low-level voltage (pins other than OSC1)	VIL	V	IOVCC = 1.65 V to 3.30 V	–0.3	-	0.20 x IOVcc	2, 3
Output high voltage (DB0-17 pins and FMARK)	VOH1	V	IOVCC = 1.65 V to 3.30 V, IOH = -0.1 mA	0.8 x IOVcc	-	-	2
Output low voltage (DB0-17 pins and FMARK)	VOL1	V	IOVCC = 1.65 V to 3.30 V, IOL = 0.1 mA	-	-	0.20 x IOVcc	2
I/O leakage current	ILi	µA	Vin = 0 to IOVcc	–1	-	1	4
Current consumption: (IOVcc-IOGND) + (Vcc-GND) Normal operation mode, 260-k color display	IOP1	µA	fosc = 376 kHz (320 lines), fFLM = 70 Hz, IOVcc = Vcc = 3.00 V, Ta = 25°C, RAM data: 18'h000000 For details, see below.	-	175	295	5, 6
Current consumption: (IOVcc-IOGND) + (Vcc-GND) 8-color mode, Sub 64-line partial display	IOP2	µA	fosc = 376 kHz (64-line partial), fFLM = 40 Hz, IOVcc = Vcc = 3.00 V, Ta = 25°C, RAM data: 18'h00000 For details, see below.	-	140	-	5, 6
Current consumption: (IOVcc-IOGND) + (Vcc-GND) Deep standby mode	IDST	µA	IOVcc = Vcc = 3.00 V, Ta = 25°C	-	0.1	1.0	5
Current consumption: (IOVcc-IOGND)+(Vcc-GND) RAM access mode 1, Normal write mode (HWM = 0)	IRAM1	mA	IOVcc = 2.40 V, Vcc = 3.00 V, tCYCW = 150 ns, Ta = 25°C, 80-8-bit I/F, TRIREG = 1'h1, consecutive RAM access during display VCM1 = 5'h1D, AP = 3'h3, BC0 = 0, FP = 5, BP = 8, gamma register: 0 (default) COL = 0 (8-color mode)	-	2.0	-	6
Current consumption: (IOVcc-IOGND)+(Vcc-GND) RAM access mode 2, High-speed write mode (HWM = 1)	IRAM2	mA	IOVcc = 2.40 V, Vcc = 3.00 V, tCYCW = 75 ns, Ta = 25°C, 80-8-bit I/F, TRIREG = 1'h1, consecutive RAM access during display VCM1 = 5'h1D, AP = 3'h3, BC0 = 0, FP = 5, BP = 8, gamma register: 0 (default) COL = 0 (8-color mode)	-	1.9	-	6

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
LCD power supply current (VCI-GND) 260k color display	I_{ci1}	mA	IOVcc1 = Vcc = 3.0V, Vci = 3.0V fosc =376kHz (320 lines), fFLM=70Hz, Ta=25°C, RAM data: 18'h0000000, REV=0, B/C=0, PxKP = 0, PxKN = 0 PxRP = 0, PxRN = 0, VxRP = 0, VxRN = 0, PxFP = 0, PxFN = 0 BT = 4'h6, VC = 3'h7, AP = 3'h3, DC0 = 3'h1, DC1 = 3'h2, VRH = 4'hA, VCM = 5'h1D, VDV = 5'h8, VCMR = 1'h1, COL = 2'h0, GON = 1, No load on the panel	—	2.8	3.3	5, 6
LCD power supply current (VCI-GND) 8-color mode (64-kine partial)	I_{ci2}	mA	IOVcc1 = Vcc = 3.0V, Vci = 3.0V fosc = 376kHz (64 line partial), fFLM = 40Hz, Ta = 25°C, RAM data: 18'h0000000, REV=0, B/C=0, PxKP = 0, PxKN = 0 PxRP = 0, PxRN = 0, VxRP = 0, VxRN = 0, PxFP = 0, PxFN = 0 BT=4'h6, VC=3'h7, AP=3'h3, DC0=3'h1, DC1=3'h2, VRH = 4'hA, VCM = 5'h1D, VDV = 5'h8, VCMR = 1'h1, COL = 2'h0, GON = 1, No load on the panel	—	1.0	—	5, 6
Output voltage dispersion	ΔVo	mV	—	—	5	—	7
Average output voltage variance	ΔVΔ	mV	—	-35	—	35	8

Step-Up Circuit Characteristics

Table 78

Item		Unit	Test Condition	Min.	Typ.	Max.	Notes
Step-up output voltage	VLOUT1	V	IOVcc = Vcc = Vcc=3.0V, Vci = Vci1 = 2.5V fosc = 376kHz, Ta = 25°C, VC = 3'h7, AP = 2'h3, BT = 3'h7, DC0 = 3'h4 (div.1/16), DC1 = 3'h4 (1/256), COL = 0, D = 2'h0, VON = 0, DIV = 2'h0, RTNI = 5'h0, FP = 4'h8, BP = 4'h8, C11 = C21 = C13 = C21 = C22 = C23 = 1[μF] / B Characteristics, VLOUT1 = VLOUT2 = VLOUT3 = VCL = 1[μF] / B Characteristics, I_{load1} = −3[mA], No load on the panel	4.57	4.84	—	—
	VLOUT2	V	IOVcc = Vcc = Vcc=3.0V, Vci = Vci1 = 2.5V fosc = 376kHz, Ta = 25°C, VC = 3'h7, AP = 2'h3, BT = 3'h7, DC0 = 3'h4 (div.1/16), DC1 = 3'h4 (1/256), COL = 0, D = 2'h0, VON = 0, DIV = 2'h0, RTNI = 5'h0, FP = 4'h8, BP = 4'h8, C11 = C21 = C13 = C21 = C22 = C23 = 1[μF] / B Characteristics, VLOUT1 = VLOUT2 = VLOUT3 = VCL = 1[μF] / B Characteristics, I_{load2} = -100[μA], No load on the panel	13.72	14.40	—	—
	VLOUT3	V	IOVcc = Vcc = Vcc=3.0V, Vci = Vci1 = 2.5V fosc = 376kHz, Ta = 25°C, VC = 3'h7, AP = 2'h3, BT = 3'h7, DC0 = 3'h4 (div.1/16), DC1 = 3'h4 (1/256), COL = 0, D = 2'h0, VON = 0, DIV = 2'h0, RTNI = 5'h0, FP = 4'h8, BP = 4'h8, C11 = C21 = C13 = C21 = C22 = C23 = 1[μF] / B Characteristics, VLOUT1 = VLOUT2 = VLOUT3 = VCL = 1[μF] / B Characteristics, I_{load3} = +100[μA], No load on the panel	-6.86	-7.13	—	—
	VCL	V	IOVcc = Vcc = Vcc=3.0V, Vci = Vci1 = 2.5V fosc = 376kHz, Ta = 25°C, VC = 3'h7, AP = 2'h3, BT = 3'h7, DC0 = 3'h4 (div.1/16), DC1 = 3'h4 (1/256), COL = 0, D = 2'h0, VON = 0, DIV = 2'h0, RTNI = 5'h0, FP = 4'h8, BP = 4'h8, C11 = C21 = C13 = C21 = C22 = C23 = 1[μF] / B Characteristics, VLOUT1 = VLOUT2 = VLOUT3 = VCL = 1[μF] / B Characteristics, I_{load4} = 200[μA], No load on the panel	-2.25	-2.30	—	—
Input voltage	Vci	V		2.5	—	3.3	—

AC Characteristics

(Vcc=2.50V ~ 3.30V, IOVcc = 1.65V ~ 3.30V, Ta = – 40°C ~ +85°C*) * see Note 1

Table 79 Clock Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
RC oscillation clock	f_{OSC}	kHz	Rf = 75kΩ	285	334	384	9

80-System Bus Interface Timing Characteristics (18/16-bit I/F)

Table 80 Normal Write Operation (HWM= "0"), IOVcc = 1.65V ~ 3.30V

Item		Symbol	Unit	Timing Diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 89	150	—	—
	Read	t_{CYCR}	ns	Figure 89	450	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 89	50	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 89	170	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 89	70	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 89	250	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 89	—	—	25
Setup time	Write (RS~CS*, WR*)	t_{AS}	ns	Figure 89	0	—	—
	Read (RS~CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 89	2	—	—
Write data setup time		t_{DSW}	ns	Figure 89	25	—	—
Write data hold time		t_H	ns	Figure 89	10	—	—
Read data delay time		t_{DDR}	ns	Figure 89	—	—	150
Read data hold time		t_{DHR}	ns	Figure 89	5	—	—

Table 81 High-Speed Write Function (HWM= "1"), IOVcc = 1.65V ~ 3.30V

Item		Symbol	Unit	Timing Diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 89	80	—	—
	Read	t_{CYCR}	ns	Figure 89	450	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 89	50	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 89	170	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 89	25	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 89	250	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 89	—	—	25
Setup time	Write (RS~CS*, WR*)	t_{AS}	ns	Figure 89	0	—	—
	Read (RS~CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 89	2	—	—
Write data setup time		t_{DSW}	ns	Figure 89	25	—	—
Write data hold time		t_H	ns	Figure 89	10	—	—
Read data delay time		t_{DDR}	ns	Figure 89	—	—	150
Read data hold time		t_{DHR}	ns	Figure 89	5	—	—

80-System Bus Interface Timing Characteristics (8-bit I/F)

Table 82 Normal/High-speed Write Function (HWM= "0/1"), IOVcc = 1.65V ~ 3.30V

Item		Symbol	Unit	Timing Diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 89	80	—	—
	Read	t_{CYCR}	ns	Figure 89	450	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 89	50	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 89	170	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 89	25	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 89	250	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 89	—	—	25
Setup time	Write (RS~CS*, WR*)	t_{AS}	ns	Figure 89	0	—	—
	Read (RS~CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 89	2	—	—
Write data setup time		t_{DSW}	ns	Figure 89	25	—	—
Write data hold time		t_{H}	ns	Figure 89	10	—	—
Read data delay time		t_{DDR}	ns	Figure 89	—	—	150
Read data hold time		t_{DHR}	ns	Figure 89	5	—	—

Serial interface Timing Characteristics

Table 83 Normal/High-Speed Write Function (HWM= "0/1"), IOVcc = 1.65V ~ 3.30V

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	t_{SCYC}	ns	Figure 90	100	-	20,000
	Read (transmitted)	t_{SCYC}	ns	Figure 90	350	-	20,000
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 90	40	-	-
	Read (transmitted)	t_{SCH}	ns	Figure 90	150	-	-
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 90	40	-	-
	Read (transmitted)	t_{SCL}	ns	Figure 90	150	-	-
Serial clock rise/fall time		t_{SCr}, t_{SCf}	ns	Figure 90	-	-	20
Chip select setup time		t_{CSU}	ns	Figure 90	20	-	-
Chip select hold time		t_{CH}	ns	Figure 90	60	-	-
Serial input data setup time		t_{SISU}	ns	Figure 90	30	-	-
Serial input data hold time		t_{SIH}	ns	Figure 90	30	-	-
Serial output data delay time		t_{SOD}	ns	Figure 90	-	-	130
Serial output data hold time		t_{SOH}	ns	Figure 90	5	-	-

Reset Timing Characteristics

Table 84 IOVcc = 1.65V ~ 3.30V

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Reset "Low" level width	t_{RES}	ms	Figure 91	1	—	—
Reset rise time	t_{rRES}	μs	Figure 91	—	—	10

RGB Interface Timing Characteristics

Table 85 18/16-Bit, 1-Transfer I/F, High-Speed Write Function (HWM= "1"), IOVcc = 1.65V ~ 3.30V

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	clocks	Figure 92	0	—	1
ENABLE setup time	tENS	ns	Figure 92	10	—	—
ENABLE hold time	tENH	ns	Figure 92	20	—	—
DOTCLK "Low" level pulse width	PW_{DL}	ns	Figure 92	40	—	—
DOTCLK "High" level pulse width	PW_{DH}	ns	Figure 92	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure 92	100	—	—
Data setup time	tPDS	ns	Figure 92	10	—	—
Data hold time	tPDH	ns	Figure 92	40	—	—
DOTCLK, VYSNC, HSYNC rise/fall time	Trgbr, trgbf	ns	Figure 92	—	—	25

Table 86 6-Bit I/F, High-Speed Write Function (HWM= "1"), IOVcc = 1.65V ~ 3.30V

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	clocks	Figure 92	0	—	1
ENABLE setup time	tENS	ns	Figure 92	10	—	—
ENABLE hold time	tENH	ns	Figure 92	25	—	—
DOTCLK "Low" level pulse width	PW_{DL}	ns	Figure 92	25	—	—
DOTCLK "High" level pulse width	PW_{DH}	ns	Figure 92	25	—	—
DOTCLK cycle time	tCYCD	ns	Figure 92	60	—	—
Data setup time	tPDS	ns	Figure 92	10	—	—
Data hold time	tPDH	ns	Figure 92	25	—	—
DOTCLK, VYSNC, HSYNC rise/fall time	Trgbr, trgbf	ns	Figure 92	—	—	25

LCD Driver Output Characteristics

Table 87

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Source driver output delay time	t_{ddS}	μs	Vcc = IOVcc = 3.0V, DDVDH = 5.5V, VREG1OUT = 5.0V, fosc = 376kHz (320 lines driven), Ta=25℃, REV=0, AP=3'h3, VRH = 4'h0, PxKPx = 3'h0, PxKNx = 3'h0 PxRNx = 3'h0, PxRPx = 3'h0, VxRNx = 5'h0, VxRPx = 5'h0, PxFPx = 2'h0, PxFNx = 2'h0, Same change from the same grayscale at all time-division source output pins, Time to reach the target voltage ±35mV from Vcom polarity inversion timing, R=10kΩ, C=20pF	—	33	—	10
Vcom output delay time	t_{ddv}	μs	Vcc = IOVcc = 3.0V, DDVDH = 5.5V, VREG1OUT = 5.0V, fosc = 376kHz (320 lines driven), Ta=25℃, REV=0, AP=3'h3, VRH = 4'h0, PxKPx = 3'h0, PxKNx = 3'h0 PxRNx = 3'h0, PxRPx = 3'h0, VxRNx = 5'h0, VxRPx = 5'h0, PxFPx = 2'h0, PxFNx = 2'h0, Time to reach the target voltage ±35mV from source V0 to V31 inversion timing, R=100Ω, C=10nF	—	33	—	11

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following figures illustrate the configurations of input, I/O, and output pins.

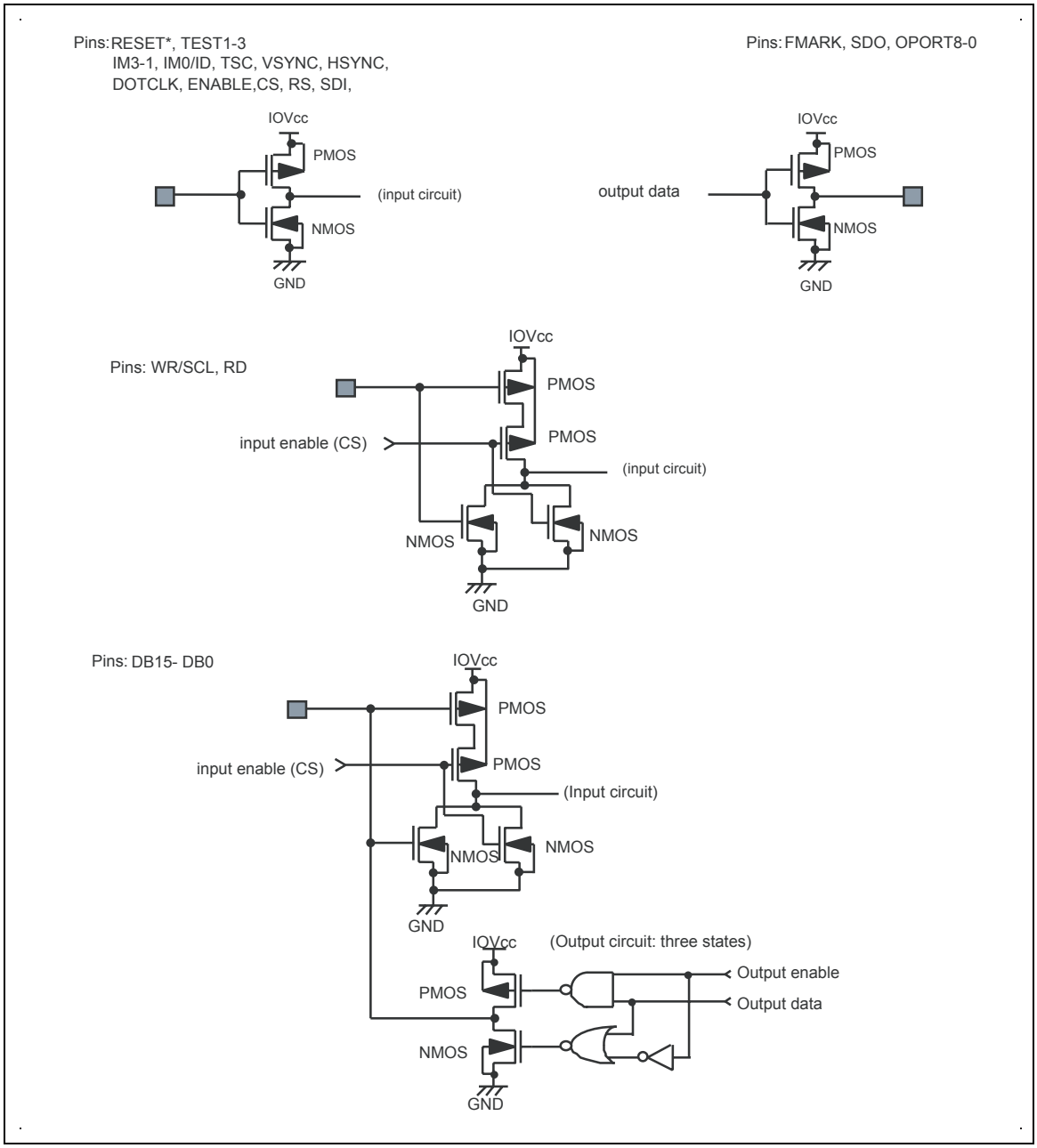


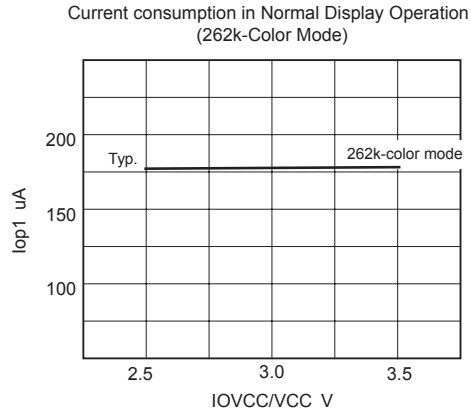
Figure 82

3. The TEST1, TEST2, and TEST5 pins must be fixed to IOGND. The TEST3 and TEST4 pins must be grounded (AGND). The IM3, IM2, IM1, IM0, and ID pins must be fixed at either IOVcc1 or IOGND1.

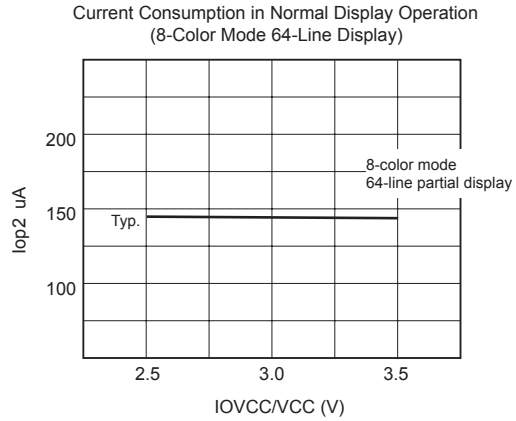
4. This excludes the current in the output-drive MOS.

5. This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is not affected by whether the CS*pin is “High” or “Low” while not accessing via interface pins.

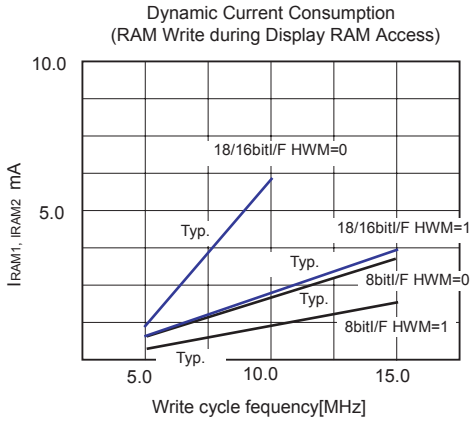
6. The relationship between voltages and the current consumption is as follows.



320 lines
Ta = 25℃, fosc = 376kHz,
fFLM = 70kHz, RAM data = 18'h00000,
COL = 0



320 lines
Ta = 25℃, fosc = 376kHz,
fFLM - 40Hz, RAM data = 18'h00000,
COL = 1,
8-color mode 64-line partial display



IOVCC = 2.4V, Vcc = 3.0V
Ta = 25℃, fosc = 376kHz

Figure 83

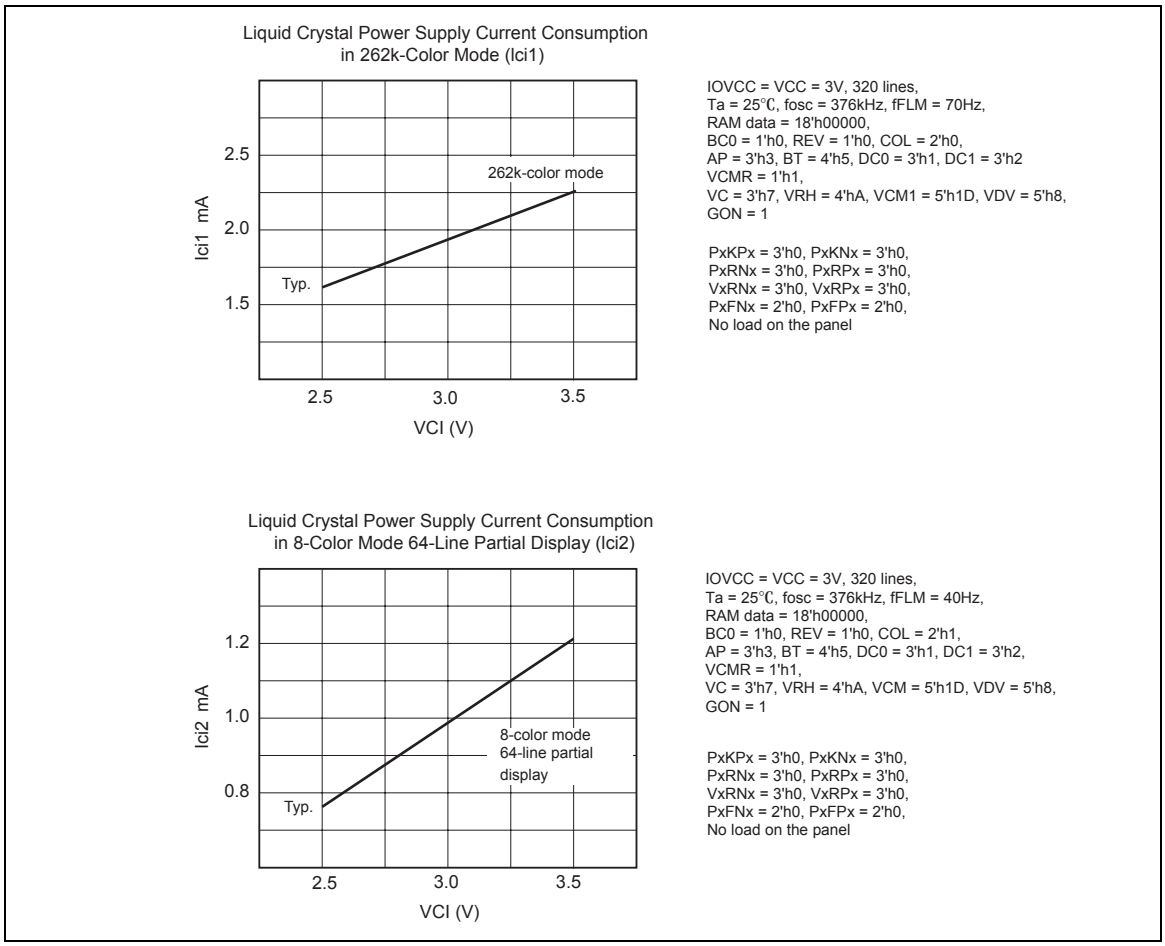


Figure 84

7. The output voltage deviation is the difference in the voltages from adjacent source pins for the same display data. This value is shown just for reference.

8. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for each chip with same display data.

9. This applies to the internal oscillator when external resistor Rf is used.

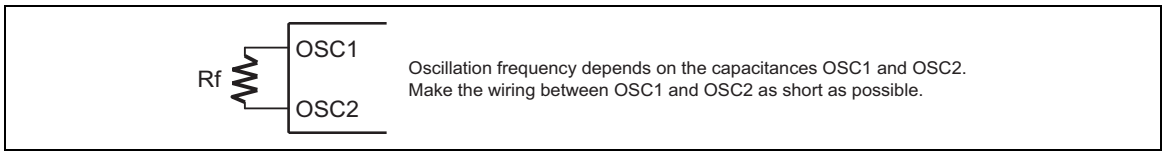


Figure 85

Table 88 Oscillation Resistance and Frequency (Reference Data)

Oscillation Resistance (kΩ)	RC Oscillation Frequency fOSC (kHz)
51	451
75	334
100	266
110	245
120	228
150	191
200	151
270	119
360	95

10. The liquid crystal driver output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality of display on the actual panel in use.

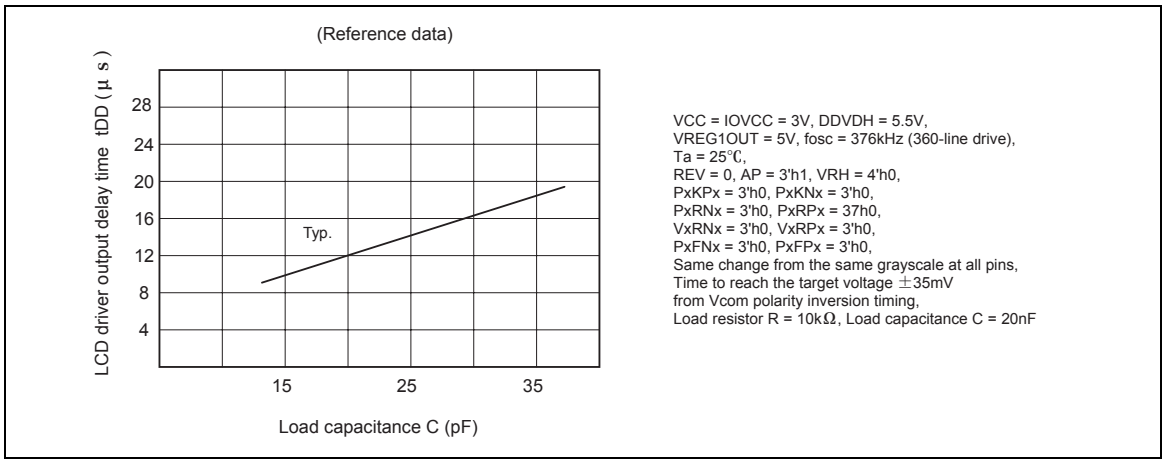


Figure 86

11. See “Load current characteristics (reference data)” for details of the characteristics of step-up circuit.

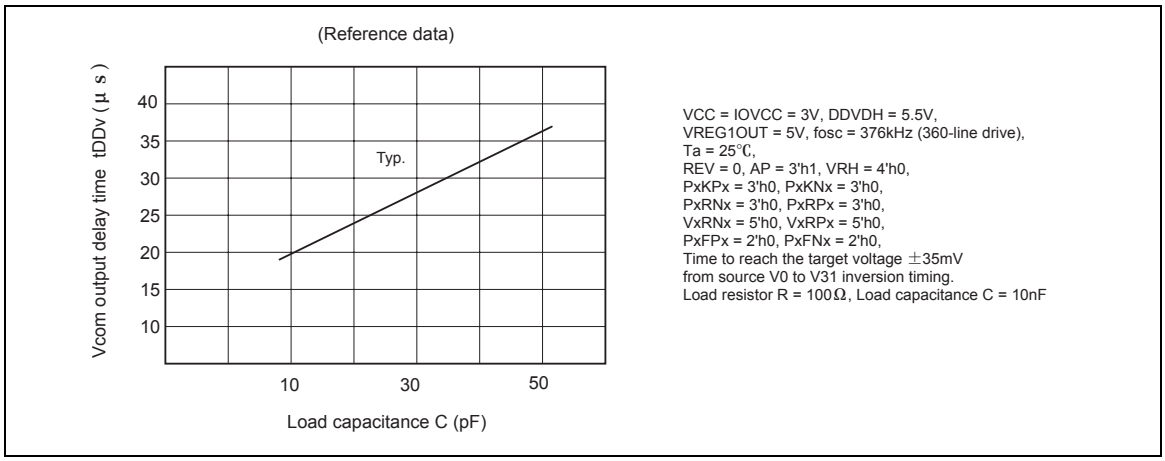


Figure 87

Test Circuits

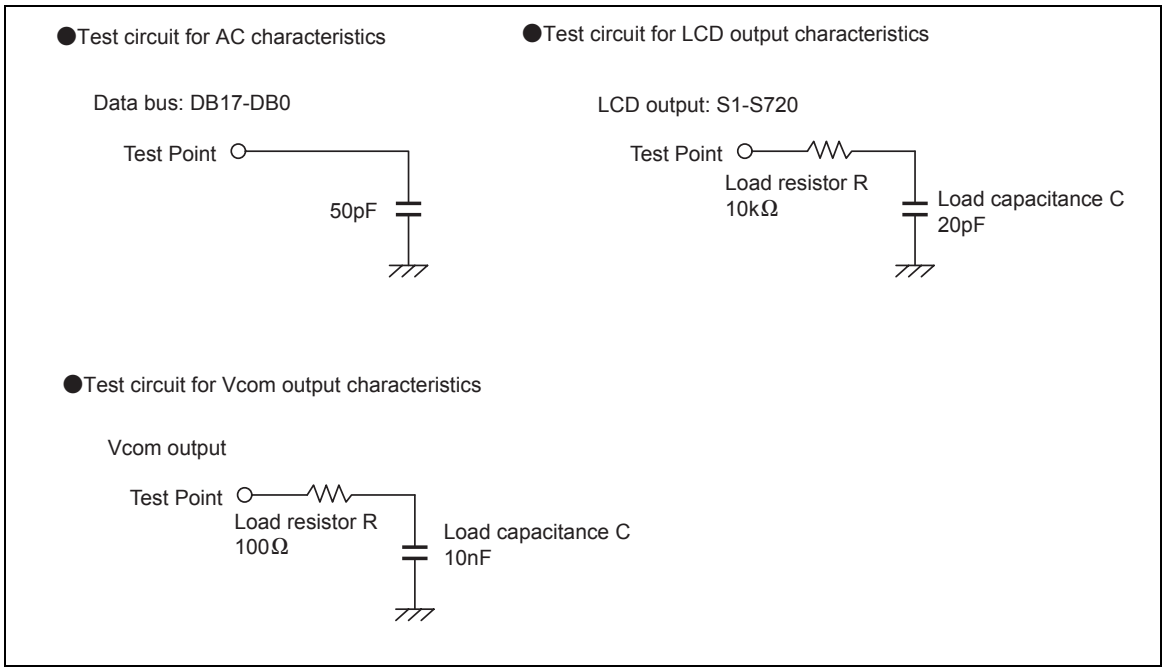
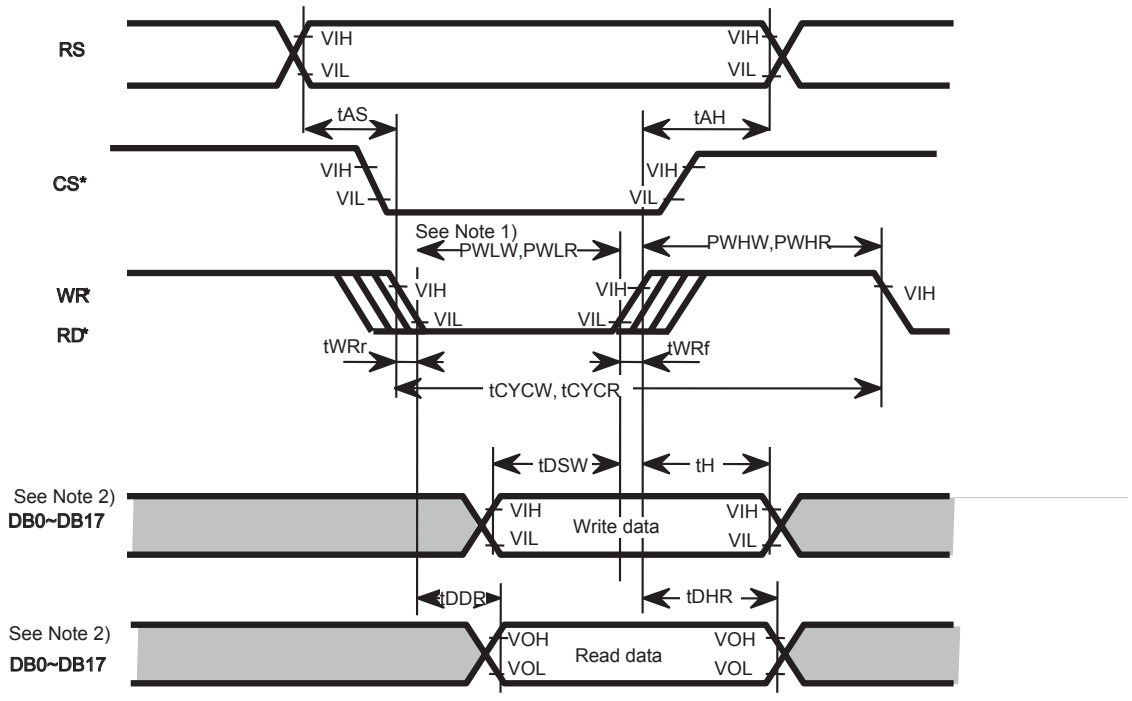


Figure 88

Timing Characteristics

80-System Bus Interface



Note 1) PWLW and PWLR are defined by the overlap period when CS* is "Low" and WR* or RD* is "Low".
Note 2) Unused DB pins must be fixed at "IOVcc" or "IOGND".

Figure 89

Clock Synchronous Serial Interface

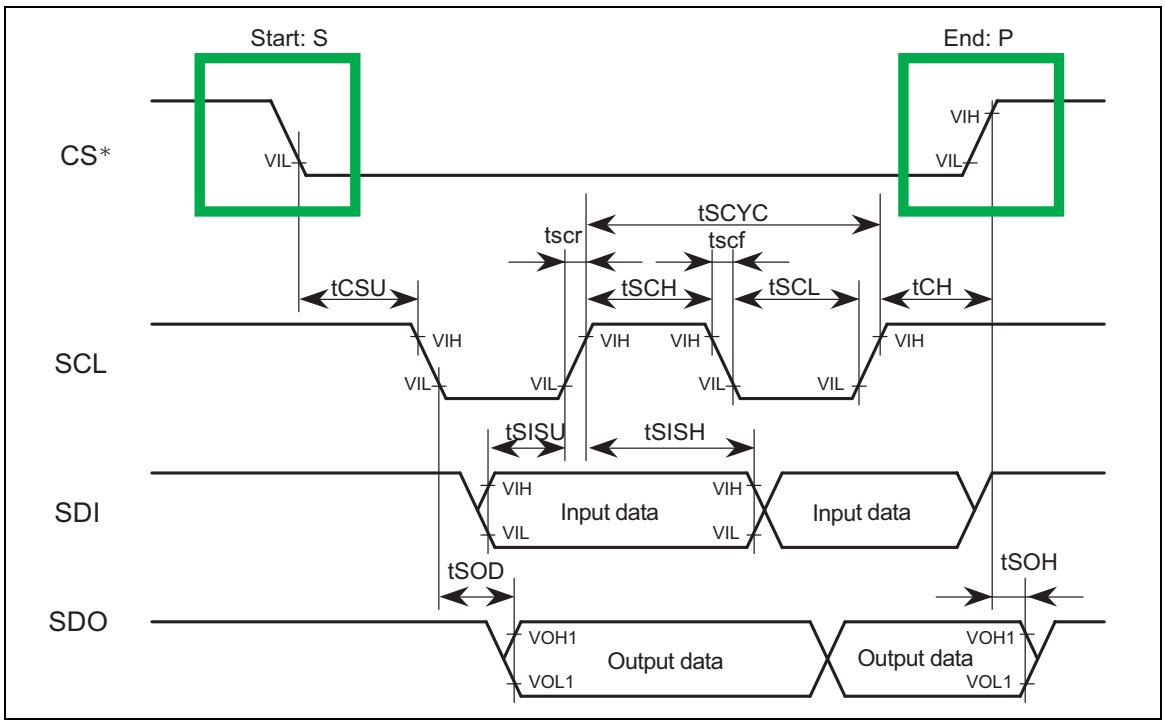


Figure 90

Reset Operation

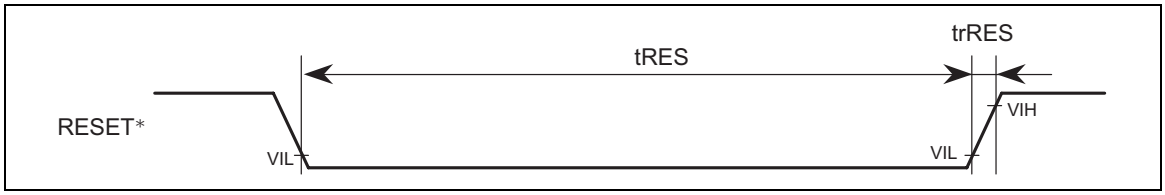


Figure 91

RGB Interface

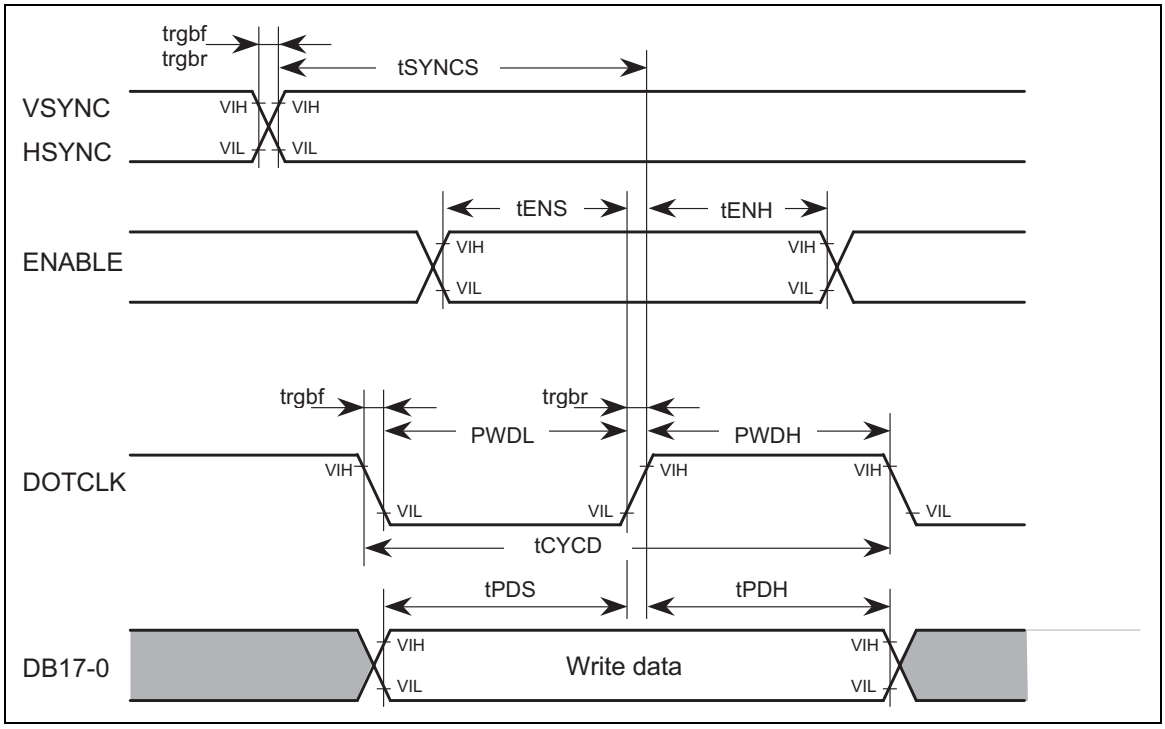


Figure 92

LCD Driver and Vcom Outputs

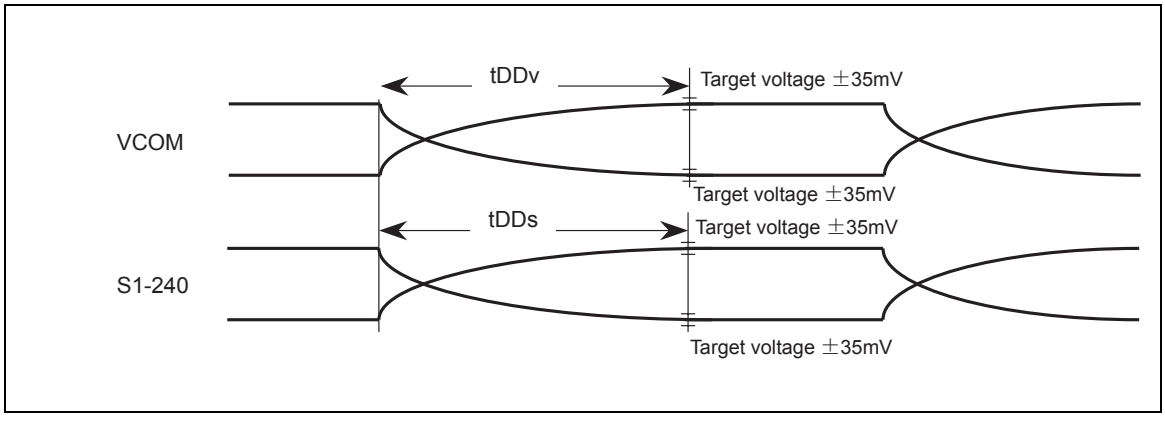


Figure 93

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.1	2005.01.05	First issue		
0.32	2005.04.15	Add pages 17 ~ 153 p.6 Add FMARK function. VGH-VGL ≤ 25V p.6, p.7 Change VGL-GND: -4.5V ~ -12.5V p.8 Changes in Block diagram (Figure 1) p.9 Error correction in Tables 2, 3 p.11 Add (6) Liquid crystal drive power supply circuit p.14 Change VLOUT3 minimum (-12.5V) p.15 Changes: VREFC, VDDTEST, IOVCCDUM1/2, TESTA5, IOGNDDUM1~3, VGLDMY1~4, TESTO1~38, TEST1/2, TEST3~5, TSC. Add VPP1~3, VCCDUM1.		
0.42	2005.08.01	p.5. Delete description about DMA transfer p.6. Changes in liquid crystal power supply voltage ranges p.7 Changes in Table 1 (VcomH, VcomL, VCL) p.8 Changes in Figure 1 (VcomR, VcomH, VcomL, VcomR) p.14 Add VCL p.15, 16 Add VcomH, VcomL, delete VcomDC, VCS, VRS. Changes in description of Vcom. p.17 Revise PAD arrangement (rev.1.2) p.19 Revise PAD coordinates table p.34 Revise Connection example (rev.1.1) p.39 Add EOR p.44 Delete SOUT1-5 from table 11 p.48 Change in Table 18 (Vcom output) p.54 Add VCL in table 27 p.57 Changes in descriptions of VCMR[0], VDV[3:0] p.59 Changes in description of WD[17:0] p.63 Changes in register R29h, table 37 p.71 Change the default value of IB4 (R90h) p.77 Changes in Output pin initial state p.131 Error correction (n line → one line) p.141, 142 Changes in Figure 72, 73 (VCL, VcomH, VcomL) p.143 Add Table 74. Changes in Table 70 p.144 Changes in Figure 74 p.145 Changes in Figure 75 p.146 Delete “standby mode”		

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.42	2005.08.01	p.147 Changes in Display ON/OFF sequences (Figure 77)		
0.43	2005.10.26	p.67 Change the default values of VEA[8:0] p.77 Add Instruction List (Rev.1.0) p.147 Error correction Power ON sequence (R17h:PSE = 1'h1) p.152 Add Absolute Maximum Ratings p.153 ~ p.167 Add Electrical characteristics		
1.0	2005.11.17	p.15 Add " When the load is on current to the maximum, VREG1OUT = 3.0V ~ (DDVDH – 0.3) is also possible." p.55 Add VCL = –3.0V (max) in Note 3. p.57 Add " When the load is on current to the maximum, VREG1OUT ≦ (DDVDH – 0.3V is also possible." p.58 Move the description of PSE from Power Control 5 to Power Control 6, add the description of BLDM. p.59 Add table 34 and the description of BLDM in Power Control 6. p.61 Write Data to GRAM → RAM Data Write, changes the sentences in the table. p.64 Read Data from GRAM → RAM Data Read, changes the sentence in the table. p.65 VCOM High Voltage → Power Control 7. p.78 Change Instruction List (14h-16h → 14h, 15h, 16h, 23h-27h → 23h-28h, 0 → Setting disabled (05h-06h, 0Bh, 0Eh, 14h, 16h, 2Ah-2Fh, 3Eh-3Fh, 54h-5Fh, 86h-8Fh, 91h, 94h, 96h, 99h-9Fh), delete F0h-FFh), add 40h-4Fh and 70h-7Fh, , 0 → BLDM, 0 → PSE(0), RAM data write/read → RAM data write/RAM data read, RAM write data (WD15-0)/RAM read data (WD15-0) → RAM data write (WD17-0)/RAM data read (RD17-0)). p.143 Change figure 72 (T.B.D. → R61505). p.144 Change figure 73 (T.B.D. → R61505). p.145 Change table 72 (HSC226 → HSL226). p.146 Add " When the load is on current to the maximum, (DDVDH – VREG1OUT) ≧ 0.3V is also possible." in Note 1 p.149 Change figure 77 (add "or R07h: 16'h0072 (BASEE = 0, VON = 1, GON = 1, DTE = 1, D = 2'h2)" in the middle "Display ON"). p.153 Delete (Target Specifications) and Note 8, Note 9 → Note 8, change table 76 ((9) → (8)). p.154 Delete (Target Specifications), change table 77 (h'00000 → 18'h000000, add "For details, see		

Rev.	Date	Contents of Modification	Drawn by	Approved by
		below" in 260k-color display and 8-color mode, add "VCM1 = 5'h1D, AP = 3'h3, BC0 = 0, FP = 5, BP = 8, gamma register: 0 (default), COL = 0 (8-color mode)" in RAM access mode 1 and 2, define Typ. (260k-colorb display, 8-color mode, Deep standby mode, RAM access mode 1 and 2) and Max. (260k-color display)).		
		p.155 Change table 77 (add (64-line partial), BT = 4'h5 → BT = 4'h6, delete "VCOMG = 1'h1, COM = 1'h1, GVD = 4'h06, GVS = 5'h14, SEN = 3'h5", define Typ. and Max. (260k-color display), define Typ. (8-color mode (64-line partial), define Min. (Average output voltage variance)).		
		p.156 Delete (Target Specifications), change table 78 (VLOUT4 → VCL, define Test Condition, Min., Max., delete 11 from Notes), change table 79 (2.5V ~ 3.1V → 2.50V ~ 3.30V, 1.65V ~ 3.1V → 1.65V ~ 3.30V, Min.: T.B.D. → 285, Typ.: 340 → 334, Max.: T.B.D. → 384).		
		p.157 Delete (Target Specifications), change table 80 (add Figure 89, Min.: 45 → 50) and table 81(add Figure 89, Min.: 75 → 80, 45 → 50).		
		p.158 Delete (Target Specifications), change table 82 (Figure 87 → Figure 89, Min.: 75 → 80, 45 → 50).		
		p.159 Delete (Target Specifications), change table 83 (Figure 88 → Figure 90) and table 84 (Figure 89 → Figure 91).		
		p.160 Delete (Target Specifications), change tables 85 and 86.(Figure 90 → Figure 92, 15 → 10 (ENABLE setup time, Data setup time)).		
		p.161 Delete (Target Specifications), define table 87 (30 → 33, T.B.D. → 33).		
		p.163 Change Note 3 (The TEST1, TEST2 pins must be grounded (IOGND1).) → The TEST 1, TEST2, and TEST 3 pins must be fixed to IOGND. The TEST3 and TEST 4 pins must be grounded (AGND)).		
		p.164 Define figure 83 (delete T.B.D.).		
		p.165 Add figure 84 (delete T.B,D,).		
		p.166 Define table 88 and figure 86 (delete T.B.D.). Delete (T.B.D.) from Note 11.		
		p.167 Add figure 87, change figure 88 (DB15 → DB17, add Test circuit for Vcom output characteristics).		
		p.170 Change figure 93 (change Vcom outputs).		
1.01	2005.12.02	p.157 Change table 81 (Min. of Write high-level pulse width: 20 → 25).		
		p.158 Change table 82 (Min. of Write high-level pulse width: 20 → 25).		

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.02	2005.12.05	p. 39 Add the description before IR. p.49 Change table 18 (the description of PTG[1:0]). p.74 Change table 47 (0 (internal clock → "Setting disabled"). p.78 Add the description of Oscillation Control. p.79 Change Instruction List (add A4h). p.149 Change figure 76 (add "RA4h: CALB = 1" and "1/osc × 8 wait"). p.150 Change figure 77 (add the description in Display ON (middle)). p.152 Change figure 79 (add "RA4h: CALB = 1" and "1/osc × wait").		
1.02a	2005.12.12	p.156 Correct table 77 (1.8 → 0.8 (Typ.)). p.157 Correct table 78 (3[mA] → −3[mA] (VLOUT1), −100[mA] → −100[μA] (VLOUT2), +100[mA] → +100[μA] (VLOUT3), 200[mA] → 200[μA] (VCL)). p.158 Correct tables 80 and 81 (t_{HWR} → t_H (Write data hold time)). p.159 Correct table 82 (t_{HWR} → t_H (Write data hold time). p.161 Correct table 86 (8-Bit → 6-Bit (title)). p.162 Correct table 87 (C = 10pF → C = 10nF (Vcom output delay time)).		
1.03	2005.12.14	p.146 Correct table 72 (HSL226 → HSC226). p.156 Correct table 77 (0.8 → 1.0 (Typ.)). p.157 Correct table 79 (IOVcc1 → IOVcc). p.158 Correct tables 80 and 81 (IOVcc1 → IOVcc). p.160 Correct tables 83 and 84 (IOVcc1 → IOVcc). p.161 Correct tables 85 and 86 (IOVcc1 → IOVcc). p.163 Correct figure 82 (IOVcc1 → IOVcc).		
1.03a	2005.12.22	p.57 Error correction (VCMR[0]: Change from IB9 to IB8)		