# **Quad 2-Input AND Gate**

# **High-Performance Silicon-Gate CMOS**

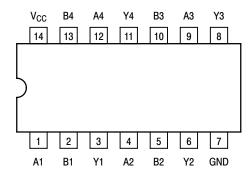
The 74HC08 is identical in pinout to the LS08. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

### **Features**

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 24 FETs or 6 Equivalent Gates
- These are Pb-Free Devices

# A1 1 2 3 Y1 A2 4 5 6 Y2 B2 5 6 Y2 A3 9 8 Y3 A4 12 11 Y4 PIN 14 = V<sub>CC</sub> PIN 7 = GND

### Pinout: 14-Lead Packages (Top View)



1



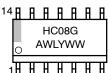
### ON Semiconductor®

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MARKING DIAGRAMS



SOIC-14 D SUFFIX CASE 751A





TSSOP-14 DT SUFFIX CASE 948G



HC08 = Device Code
A = Assembly Location

WL or L = Wafer Lot Y = Year WW or W = Work Week G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### **FUNCTION TABLE**

Inp	uts	Output
Α	В	Υ
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

### **MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	$-$ 0.5 to $V_{CC}$ + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)		6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	٧
T <sub>A</sub>	Operating Temperature Range, All Package Types		+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise/Fall Time $V_{CC} = 2.0 \text{ V}$ (Figure 1) $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0	1000 500 400	ns

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
74HC08DR2G	SOIC-14 (Pb-Free)	2500/Tape & Reel
74HC08DTR2G	TSSOP-14*	

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>This package is inherently Pb-Free.

# DC CHARACTERISTICS (Voltages Referenced to GND)

			V <sub>CC</sub> Guaranteed Limit		nit		
Symbol	Parameter	Condition	(V)	-55 to 25°C	≤ <b>85</b> °C	≤125°C	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage	$V_{out} = 0.1V \text{ or } V_{CC} - 0.1V$ $ I_{out}  \le 20 \mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	>
V <sub>IL</sub>	Maximum Low-Level Input Voltage	$V_{out} = 0.1V \text{ or } V_{CC} - 0.1V$ $ I_{out}  \le 20\mu\text{A}$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} \qquad  I_{\text{out}}  \le 2.4 \text{mA} \\  I_{\text{out}}  \le 4.0 \text{mA} \\  I_{\text{out}}  \le 5.2 \text{mA}$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	<b>V</b>
		$V_{in} = V_{IH} \text{ or } V_{IL} \qquad \begin{aligned}  I_{out}  &\leq 2.4 \text{mA} \\  I_{out}  &\leq 4.0 \text{mA} \\  I_{out}  &\leq 5.2 \text{mA} \end{aligned}$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	6.0	2.0	20	40	μΑ

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## AC CHARACTERISTICS ( $C_L = 50 pF$ , Input $t_r = t_f = 6 ns$ )

		v <sub>cc</sub>	Guaranteed Limit			
Symbol	Parameter	(V)	-55 to 25°C	≤85°C	≤125°C	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V		ĺ
$C_{PD}$	Power Dissipation Capacitance (Per Buffer)*	20	pF	l

<sup>\*</sup> Used to determine the no–load dynamic power consumption:  $P_D = C_{PD} \, V_{CC}^2 f + I_{CC} \, V_{CC}$ . For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

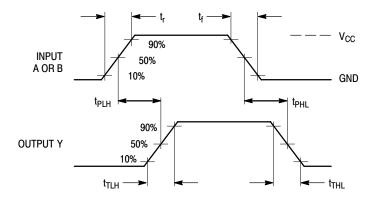
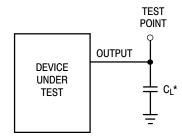


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

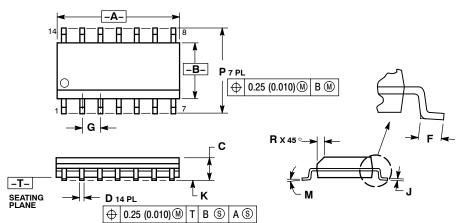
Figure 2. Test Circuit



Figure 3. Expanded Logic Diagram (1/4 of the Device)

### PACKAGE DIMENSIONS

SOIC-14 CASE 751A-03 **ISSUE H** 



- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

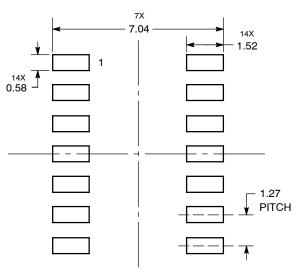
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
М	0 °	7 °	0 °	7 °
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010 0.019	

### **SOLDERING FOOTPRINT\***

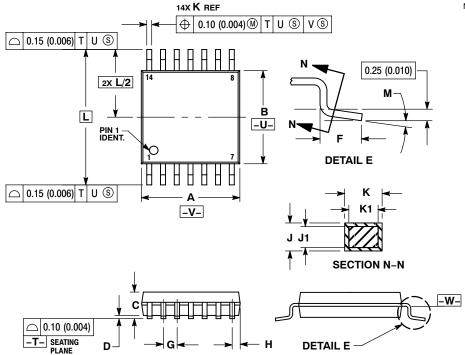


DIMENSIONS: MILLIMETERS

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### PACKAGE DIMENSIONS

### TSSOP-14 CASE 948G-01 ISSUE B



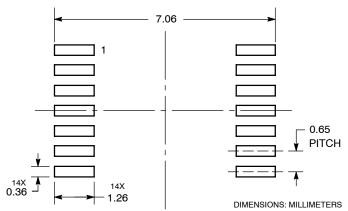
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER

  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
     CONTROLLING DIMENSION: MILLIMETER.
     DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
     DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  - NOT EXCEED 0.25 (0.010) PER SIDE.

    5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
    6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
    7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40	BSC	0.252 BSC		
М	0 °	8 °	0 °	8 °	

### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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