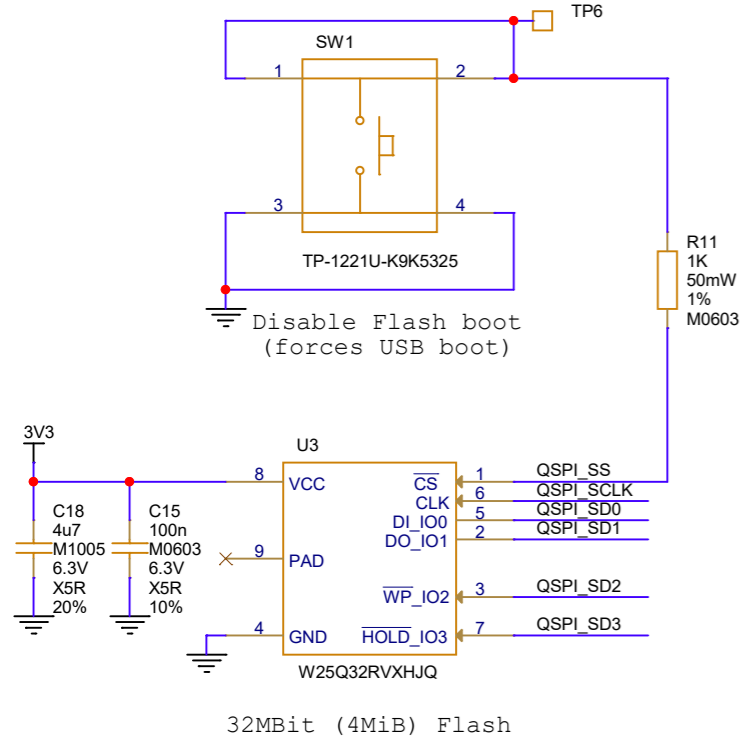
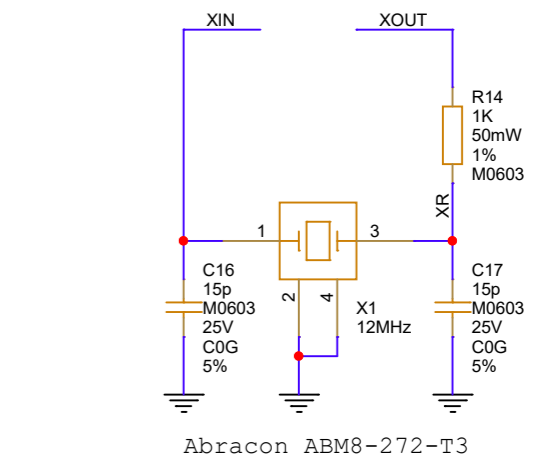
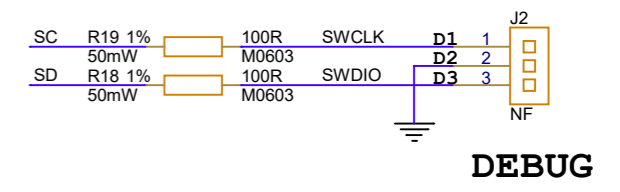
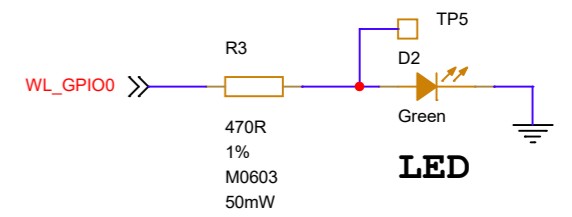
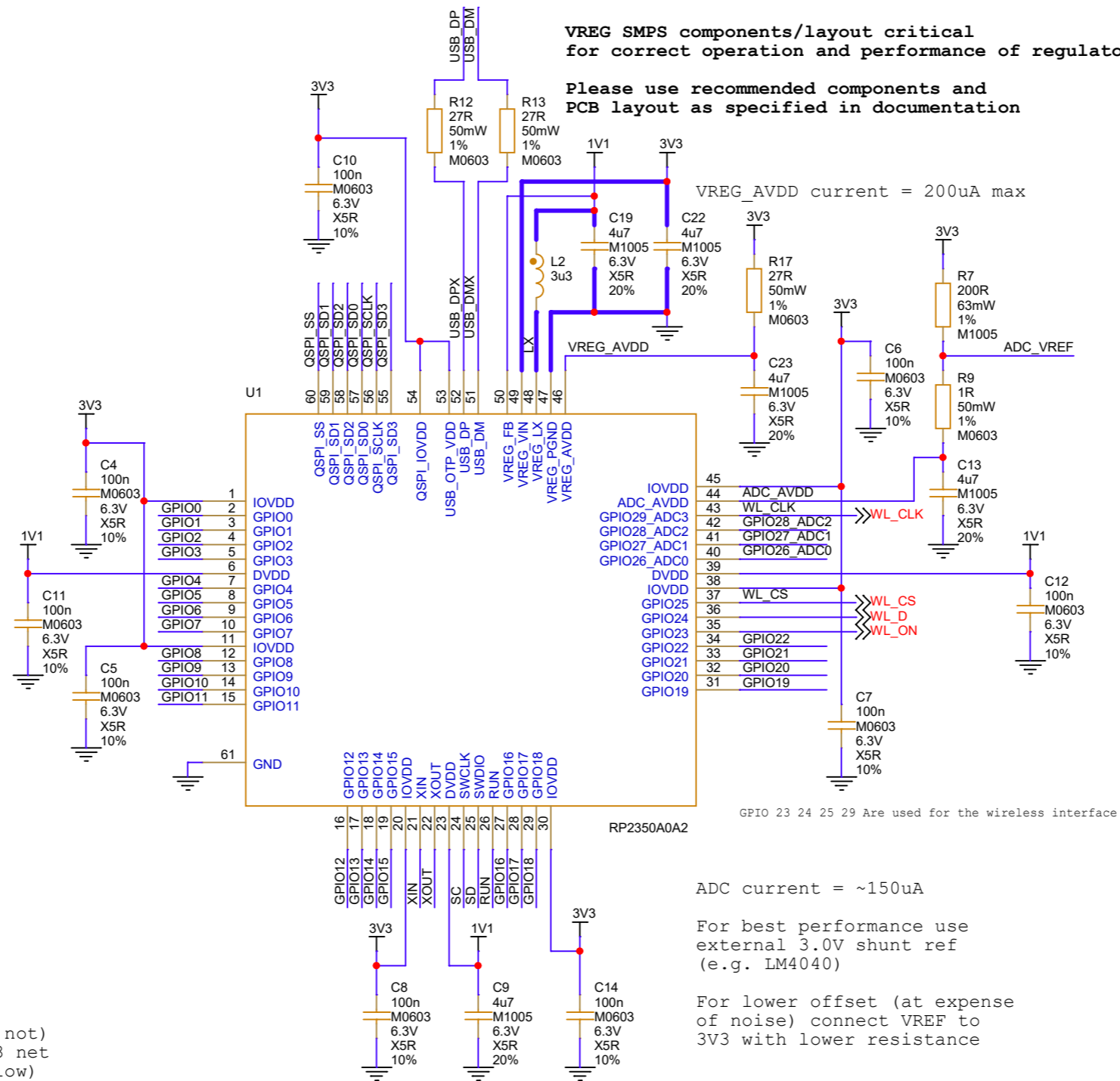


BOOTSEL

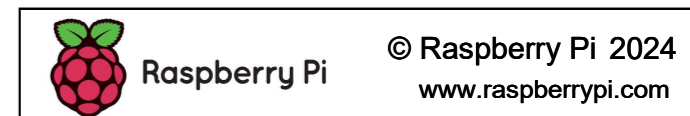


VREG SMPS components/layout critical for correct operation and performance of regulator

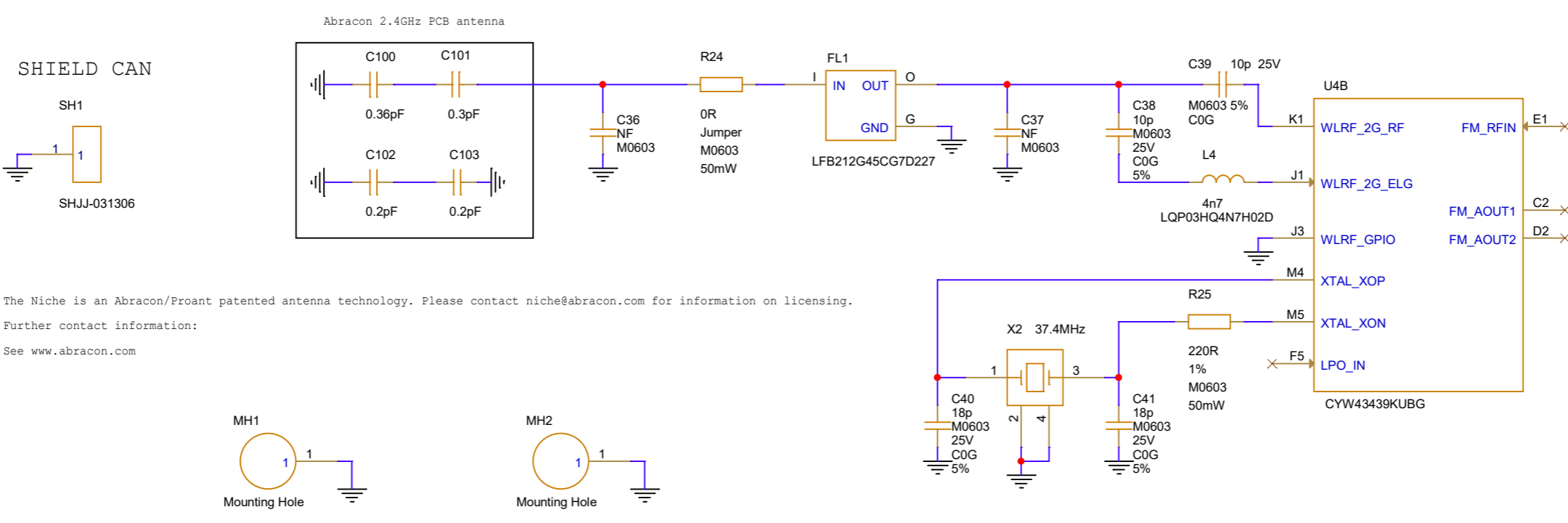
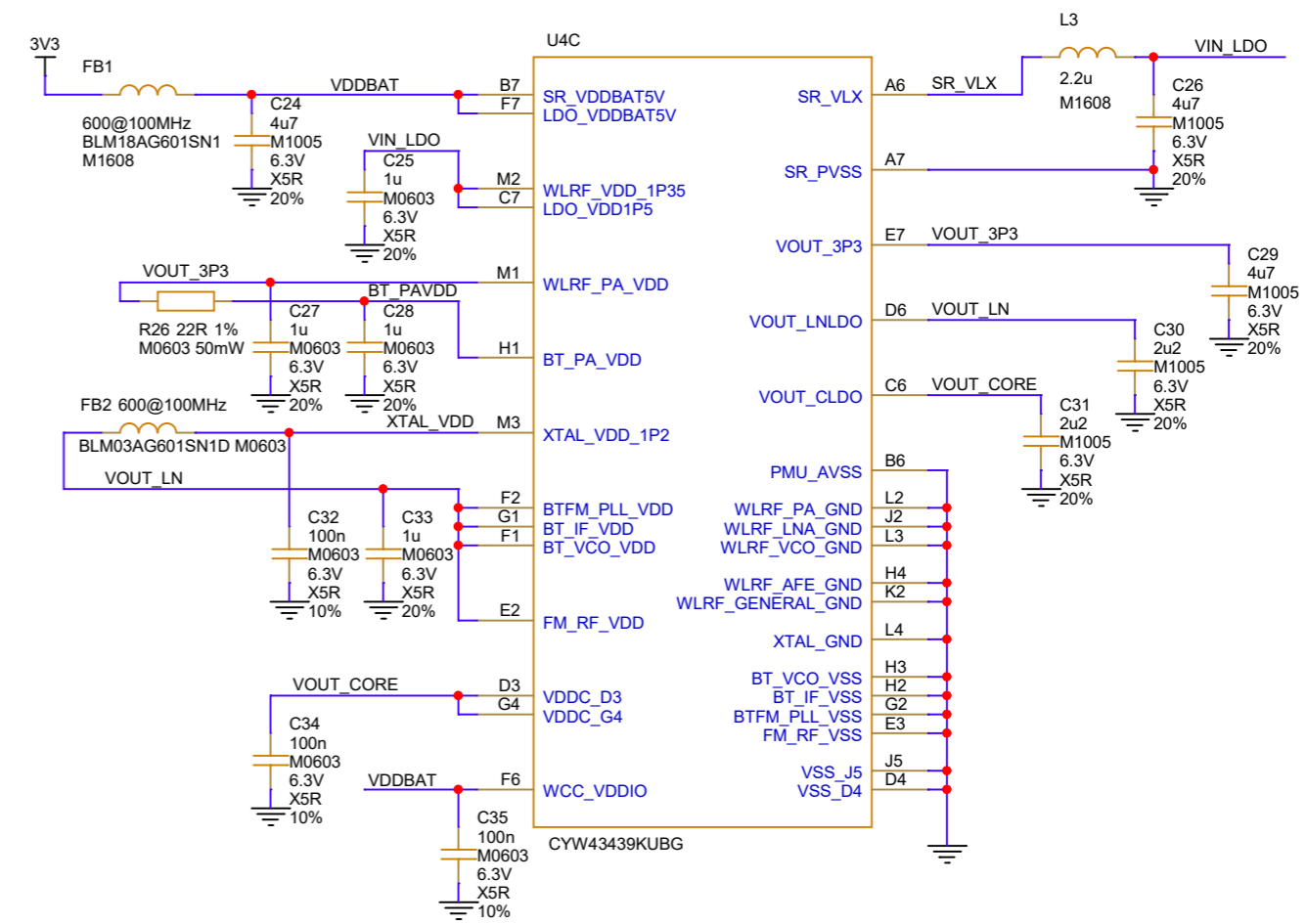
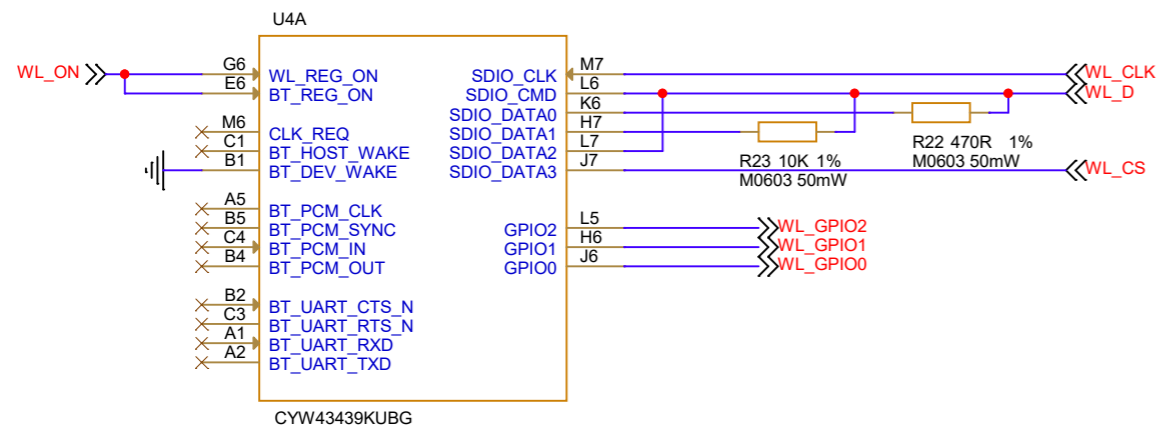
Please use recommended components and PCB layout as specified in documentation



ADC GPIO pins have diode to VDDIO (other GPIO do not)
 FET stops leakage through ADC3 pin diode into 3V3 net when 3V3 supply is off (VSYS present but 3V3_EN low)



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Size A3	Ref RPI-PICO2W	Rev 2	
Date: Friday, July 19, 2024		Sheet 2 of 2	