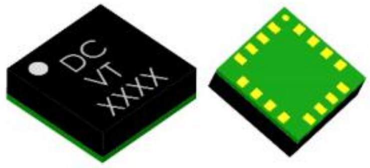
Three-Axis Magnetic Sensor
VCM5883L

Datasheet

The VCM5883L is a three-axis magnetic sensor with very low power consumption developed specifically for Drone Nevigation. This surface-mount, small sized chip has integrated magnetic sensors with signal condition ASIC, it offers the advantages of low noise, high accuracy, low power consumption, offset cancellation.



The VCM5883L is based on Anisotropic Magneto-Resistive (AMR) and CMOS technology, Linear three axis magnetic sensor along with custom-designed 16-bit ADC and power management ASIC, it provides digital signal with I²C serial bus.

The VCM5883L is in a 3x3x0.9mm^3 surface mount 16-pin land grid array (LGA) package.

FEATURES	BENEFIT
3-Axis Magneto-Resistive Sensors in a 3x3x0.9 mm^3 Land Grid Array Package (LGA), guaranteed to operate over an extended temperature range of -40°C to +85°C.	Small Size for Highly Integrated Products. Signals Have Been Digitized And Calibrated.
16 Bit ADC With Low Noise AMR Sensors Achieves 2 Milli-Gauss Field Resolution	Enables 1° to 2° Degree Compass Heading Accuracy , Allows for Navigation and LBS Applications
Wide Magnetic Field Range (±8 Gauss)	Maximizes Sensor's Full Dynamic Range and Resolution
I^{2}C (Standard ,Fast Modes) Interface.	High Speed Digital Output
Low Operation Voltage (2.16V To 3.6V) and Low Power Consumption	Compatible with Battery Powered Applications
Lead Free Package Construction	RoHS Compliance
Software And Algorithm Support Available	Compassing Heading, Hard Iron, Soft Iron, and Auto Calibration Libraries Available

1 INTERNAL SCHEMATIC DIAGRAM

1.1 Internal Schematic Diagram

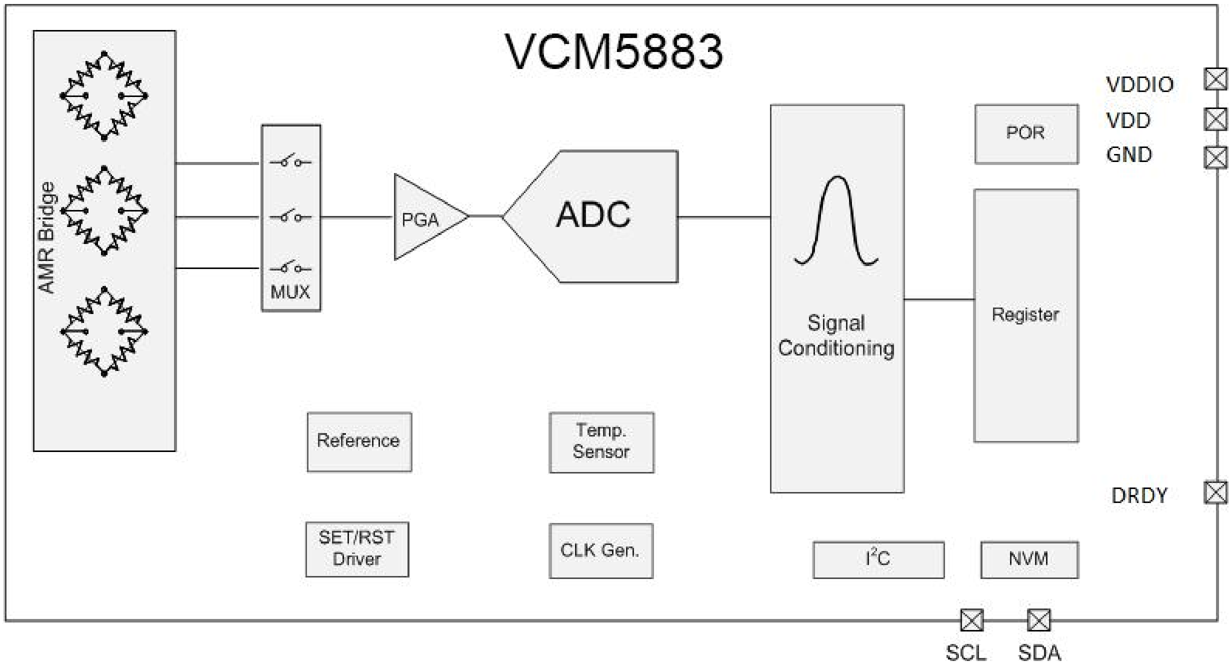


Figure 1. Block Diagram

Table 1. Block Function

Block	Function
AMR Bridge	3 axis magnetic sensor
MUX	Multiplexer for sensor channels
PGA	Programmable gain amplifier for sensor signals
ADC	16bit Analog-to-Digital converter
Signal Conditioning	Digital blocks for magnetic signal calibration and compensation
I^2C	Interface logic data I/O
NVM	Non-Volatile memory for calibrated parameters
SET/RST Driver	Internal driver to initialize magnetic sensor
Reference	Voltage/Current reference for internal biasing
Clock Gen.	Internal oscillator for internal operation
POR	Power on reset
Temperature Sensor	Temperature sensor for internal sensitivity/offset compensation, and temperature output

2 SPECIFICATIONS AND I/O CHARACTERISTICS

2.1 Product Specifications

Table 2. Specifications (* Tested and specified at 25°C except stated otherwise.)

Parameter	Conditions		Min	Typ	Max	Unit
Supply Voltage	VDD		2.16		3.6	V
I/O Voltage	VDDIO		1.65		3.6	V
Standby	Total current on VDD and VDDIO			5		uA
Supply Current	Normal Mode	ODR = 10Hz, A=0Dh		150		μA
		ODR = 50Hz, A=09h		350		uA
		ODR = 100Hz, A=05h		500		uA
	A=01h,B=0x03h,ODR=200Hz			1000		uA
Sensor Field Range	Full Scale		-8		+8	Gauss
Sensitivity [1]	Field Range = ±8G			3000		LSB/G
Linearity (Best fit linear curve)	Field Range = ±8G			0.1		%FS
Hysteresis	All Ranges			0.1		%FS
Cross Axis Sensitivity	Cross field = 1 Gauss, Happlied = ±2 Gauss			0.1		%/G
Offset				±10		mG
Sensitivity Tempco	Ta = -40℃~85℃			±0.05		%/℃
Total Peak to Peak Noise				1		mG
Digital Resolution	Change with Gain		0.1		1.0	mGauss
Field Resolution	Standard deviation 100 Data, FS ±2G			2		mGauss
Output Data Rate	Programmable. 10Hz/50Hz/100Hz/200Hz		10		200	Samples/ sec
X-Y-Z Orthogonality	Sensitivity Directions			90±1		degree
Operating Temperature			-40		85	℃
ESD	HB Model		5500			V
	Charge Device Model		750			

Note [1]: Sensitivity is calibrated at zero field, it is slightly decreased at high fields.

2.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings (Tested at 25°C except stated otherwise.)

Parameter	MIN.	MAX.	Units
VDDIO	-0.3	5.4	V
VDD	-0.3	5.4	V
Storage Temperature	-40	125	°C
Exposed to Magnetic Field (all directions)		50000	Gauss
Reflow Classification	MSL 3, 260°C Peak Temperature		

2.3 I/O Characteristics

Table 4. I/O Characteristics

Parameter	Symbol	Pin	Condition	Min.	TYP.	Max.	Unit
Voltage Input High Level 1	$V_{IH}1$	SDA, SCL		0.7*VDDIO		VDDIO+0.3	V
Voltage Input Low Level 1	$V_{IL}1$	SDA, SCL		-0.3		0.3*VDDIO	V
Voltage Output High Level	V_{OH}	INT	Output Current ≥-100uA	0.8*VDDIO			V
Voltage Output Low Level	V_{OL}	INT, SDA	Output Current ≤100uA(INT) Output Current ≤1mA (SDA)			0.2*VDDIO	V

3 Application Examples

3.2 Measurement Example

- ✧ Write register 0AH by 0x0xh.
- ✧ Read data register 00H ~ 05H.

3.3 Standby Example

- ✧ Write Register 0AH by 0x00

3.4 Soft Reset Example

- ✧ Write Register 0BH by 0x80

4 I2C COMMUNICATION PROTOCOL

4.1 I2C Timings

Below table and graph describe the I^{2}C communication protocol times

Table 5. I2C Timings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock	f_{scl}		0		400	kHz
SCL Low Period	t_{low}		1			µs
SCL High Period	t_{high}		1			µs
SDA Setup Time	t_{sudat}		0.1			µs
SDA Hold Time	t_{hddat}		0		0.9	µs
Start Hold Time	t_{hdsta}		0.6			µs
Start Setup Time	t_{susta}		0.6			µs
Stop Setup Time	t_{susto}		0.6			µs
New Transmission Time	t_{buf}		1.3			µs
Rise Time	t_r					µs
Fall Time	t_f					µs

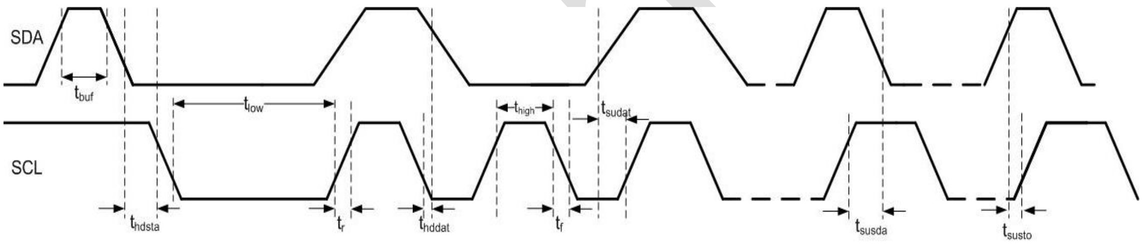


Figure 2. I2C Timing Diagram

4.2 I2C R/W Operation

4.2.1 Abbreviation

Table 6. Abbreviation

SACK	Acknowledged by slave
MACK	Acknowledged by master
NACK	Not acknowledged by master
RW	Read/Write

4.2.2 Start/Stop/ACK

START: Data transmission begins with a high to transition on SDA while SCL is held high. Once I^{2}C transmission starts, the bus is considered busy.
STOP: STOP condition is a low to high transition on SDA line while SCL is held high.
ACK: Each byte of data transferred must be acknowledged. The transmitter must release the SDA line during the acknowledge pulse while the receiver mush then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.
NACK: If the receiver doesn't pull down the SDA line during the high period of the acknowledge clock cycle, it's recognized as NACK by the transmitter.

4.2.3 I2C Address

The default I^{2}C Address is OC: 0001100.
More I^{2}C Address can be obtained through factory change.

4.2.4 I2C Write

I^{2}C write sequence begins with start condition generated by master followed by 7 bits slave address and a write bit (R/W=0). The slave sends an acknowledge bit (ACK=0) and releases the bus. The master sends the one byte register address. The slave again acknowledges the transmission and waits for 8 bits data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Table 7. I2C Write

START	Slave Address							R W	SACK	Register Address (0x0A)								SACK	Data (0x41)								SACK	STOP
	0	0	0	1	1	0	0	0		0	0	0	0	1	0	1	0		0	0	0	0	0	0	0	1		

4.2.5 I2C Read

I^{2}C write sequence consists of a one-byte I^{2}C write phase followed by the I^{2}C read phase. A start condition must be generated between two phase. The I^{2}C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (R/W=1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.
The register address is automatically incremented and more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the current I^{2}C write command.

Table 8. I2C Read

START	Slave Address							R W	SACK	Register Address (0x00)								SACK										
	0	0	0	1	1	0	0	0		0	0	0	0	0	0	0	0											
START	Slave Address							R W	SACK	Data (0x00)								MACK	Data (0x01)									
	0	0	0	1	1	0	0	1		0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	1		
MACK	Data (0x02)								MACK	…………………………… …….								MACK	Data (0x07)								NACK	STOP
	0	0	0	0	0	0	1	0		…………………………… …….									0	0	0	0	0	1	1	1		

5 REGISTERS

5.1 Register Map

The table below provides a list of the 8-bit registers embedded in the device and their respective function and addresses.

Table 9. Register Map

Addr.	7	6	5	4	3	2	1	0	Access
00H	Data Output X LSB Register XOUT[7:0]								Read only
01H	Data Output X MSB Register XOUT[15:8]								Read only
02H	Data Output Y LSB Register YOUT[7:0]								Read only
03H	Data Output Y MSB Register YOUT[15:8]								Read only
04H	Data Output Z LSB Register ZOUT[7:0]								Read only
05H	Data Output Z MSB Register ZOUT[15:8]								Read only
0AH					ODR[1:0]			MODE	R/W
0BH	SOFT_ RST						SET/RESET MODE		R/W
0CH	Chip ID								Read only

*** Warning: All undefined bits in the register must write '0', if it is written '1', the function and performance of the chip will be greatly affected , even the chip may be damaged.**

5.2 Register Definition

5.2.1 Output Data Register

Registers 00H ~ 05H store the measurement data from each axis magnetic sensor in continuous-measurement. In the Normal measurement mode, the output data is refreshed periodically based on the data update rate ODR setup in control register 1. The data stays the same, regardless of reading status through I^{2}C, until new data replaces them. Each axis has 16 bit data width in 2's complement, i.e., MSB of 01H/03H/05H indicates the sign of each axis.The output data of each channel saturates between -32768 and 32768.

Table 10. Output Data Register

Addr.	7	6	5	4	3	2	1	0
00H	Data Output X LSB Register XOUT[7:0]							
01H	Data Output X MSB Register XOUT[15:8]							
02H	Data Output Y LSB Register YOUT[7:0]							
03H	Data Output Y MSB Register YOUT[15:8]							
04H	Data Output Z LSB Register ZOUT[7:0]							
05H	Data Output Z MSB Register ZOUT[15:8]							

5.2.2 Control Registers

Two 8-bits registers are used to control the device configurations.
Control register 1 is located in address 0BH, it set soft reset(SOFT_RST), enable the feature of automatic set/reset.

Control register 2 is located in address 0AH. it sets the operational modes (MODE) and the output data rates (ODR).

The ODR bit can transfer data rates of output in the device, the four output data rates are 10Hz、50Hz、100Hz and 200Hz. The output data rates correspond to the measurement cycle frequency one by one. By setting the ODR, the power consumption of the device decreases with the decrease of output data rates. The default ODR after Power-on-Reset (POR) is 200Hz.

The MODE bit can transfer mode of operations in the device, the two modes are Standby and Normal. The Standby mode only support the basic functions of analog and digital without any measurement. The Normal mode runs in the measurement cycle state, and the cycle frequency is controlled by the ODR bit. The default mode after Power-on-Reset (POR) is standby. There is no any restriction in the transferring between the modes.

SET/RESET function is realized by generating pulse current between sensors S/R+ and S/R- .When a set pulse is applied, the component of the output and external magnetic field strength on the sensitive axis of the magnetometer is a straight line with a positive slope. When a reset pulse is applied, the component of the output and external magnetic field strength on the sensitive axis of the magnetometer is a straight line with a negative slope. All in all , the function of SET/RESET is to restore the initial state of AMR built-in magnetic field.

Table 12. Control Register

Control Register 1	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	0BH	SOFT_RST						SET/RESET	
	Reg.	**Definition**		**0**			**1**		
	SOFT_RST	Reset registers to default value		Normal			Reset and Clear		
	Reg.	**Definition**		**00**	**01**		**10**	**11**	
	SET/RESET	SET/RESET mode		SET/RESET	SET		NO SET/RESET	Reserve	
Control Register 2	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	0AH					ODR[1:0]			MODE
	Reg.	**Definition**		**0**			**1**		
	Mode	Mode Control		Standby			Normal		
	Reg.	**Definition**		**00 (default)**	**01**		**10**	**11**	
	ODR	Output data rates		200Hz	100Hz		50Hz	10Hz	

Note : During initialization , register 0AH(bit7~bit4) must be written 0100b

Soft Reset can be done by changing the register SOFT_RST to set. Soft reset can be invoked at any time of any mode. For example, if soft reset occurs at the middle of Normal mode reading, VCM5883L immediately switches to standby mode due to all registers are reset to “00” in default.

SOFT_RST: “0”: Normal“1”: Soft reset, restore default value of all registers.

5.2.3 Chip ID Register

This register is chip identification register. It returns 0x82.

Table 13. Chip ID Register

Addr.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0CH	1	0	0	0	0	0	1	0

6 EXTERNAL CONNECTION

6.1 Dual Supply Connection

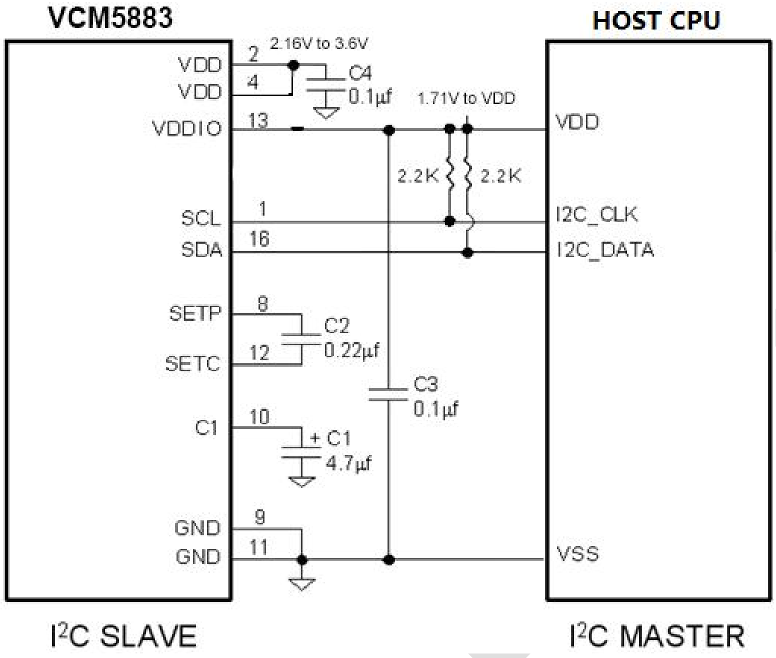


Figure 3. Dual Supply Connection

6.2 Single Supply connection

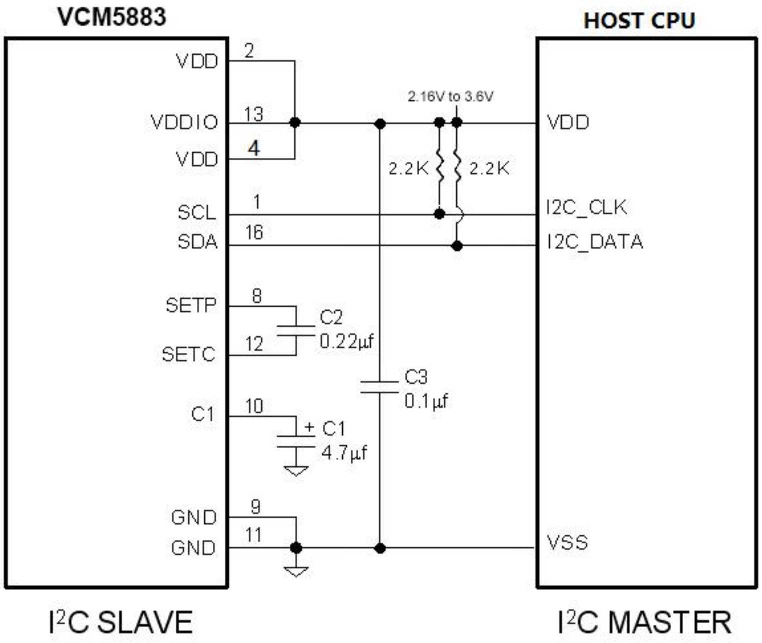


Figure 4. Single Supply Connection

6.3 Mounting Considerations

The following is the recommend printed circuit board (PCB) footprint for the VCM5883L. Due to the fine pitch of the pads, the footprint should be properly centered in the PCB.

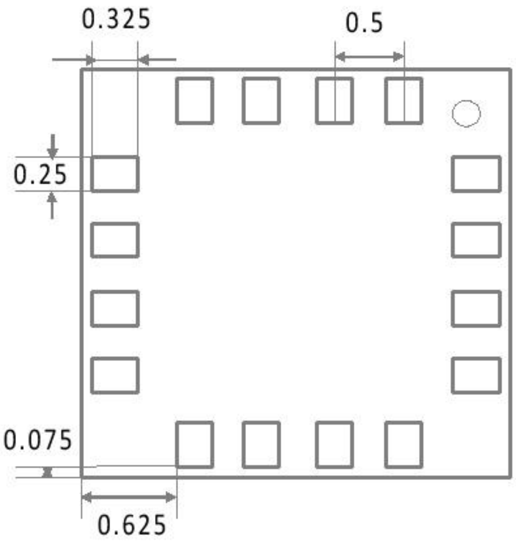


Figure 5. VCM5883L PCB footprint

6.4 Layout Considerations

Besides keeping all components that may contain ferrous materials (nickel, etc.) away from the sensor on both sides of the PCB, it is also recommended that there is no conducting copper line under/near the sensor in any of the PCB layers.

6.4.1 Solder Paste

A 4 mil stencil and 100% paste coverage is recommended for the electrical contact pads.

6.4.2 Reflow Assembly

This device is classified as MSL 3 with 260°C peak reflow temperature. As specified by JEDEC, parts with an MSL 3 rating require baking prior to soldering, if the part is not kept in a continuously dry (< 10% RH) environment before assembly. Reference IPC/JEDEC standard J-STD-033 for additional information.

No special reflow profile is required for VCM5883L, which is compatible with lead eutectic and lead-free solder paste reflow profiles. VTRAN recommends adopting solder paste manufacturer's guidelines. Hand soldering is not recommended.

6.4.3 External Capacitors

The external capacitors C1 should be ceramic type with low ESR characteristics. The exact ESR value is not critical, but values less than 200 milli-ohms are recommended. Reservoir capacitor C1 is nominally 4.7 μF in capacitance, with the set/reset capacitor C2 nominally 0.22 μF in capacitance. Low ESR characteristics may not be in many small SMT ceramic capacitors (0402), so be prepared to up-size the capacitors to gain low ESR characteristics.

7 PACKAGE PIN CONFIGURATIONS

7.1 Package 3-D View

Arrow indicates direction of magnetic field that generates a negative output reading in normal measurement configuration.

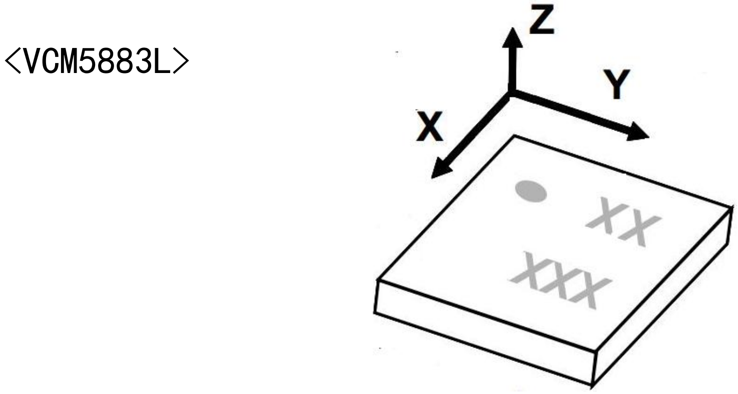


Figure 6. Package 3-D View

Table 14. Pin Configurations

PIN No.	PIN NAME	Function
1	SCL	Serial Clock – I^{2}C Master/Slave Clock
2	VDD	Power Supply (2.16V to 3.6V)
3	NC	Not to be Connected
4	VDD	Power supply
5	NC	Not to be Connected
6	NC	Not to be Connected
7	NC	Not to be Connected
8	SETP	Set/Reset Strap Positive – S/R Capacitor (C2) Connection
9	GND	Supply Ground
10	C1	Reservoir Capacitor (C1) Connection
11	GND	Supply Ground
12	SETC	S/R Capacitor (C2) Connection – Driver Side
13	VDDIO	IO Power Supply (1.71V to VDD)
14	NC	Not to be Connected
15	NC	Not to be Connected
16	SDA	Serial Data – I^{2}C Master/Slave Data

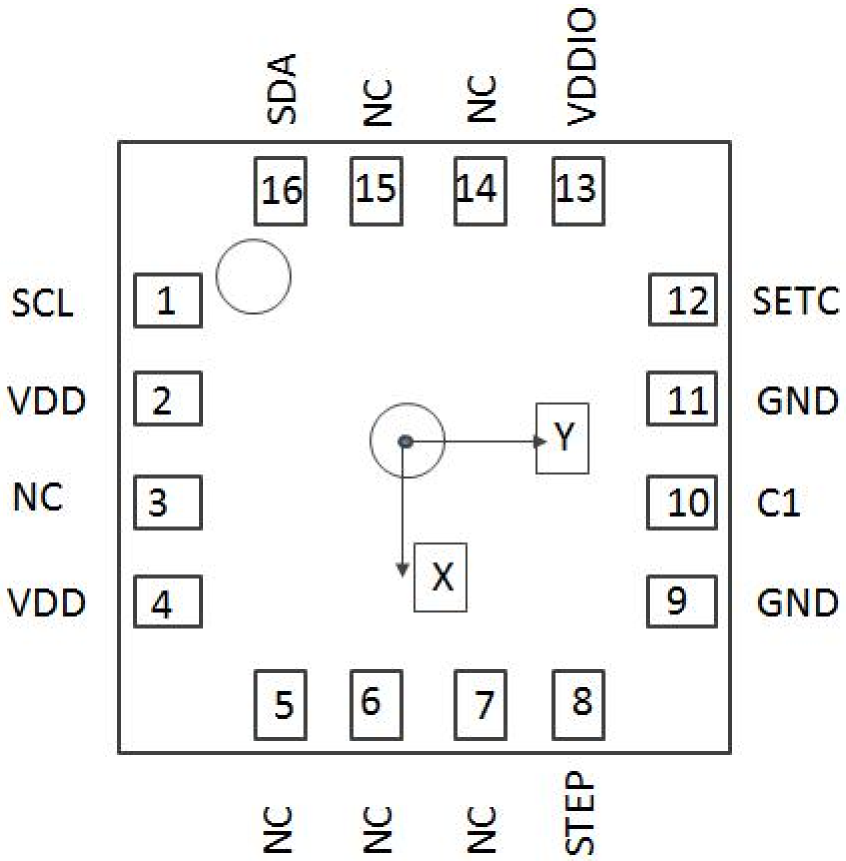


Figure 7. TOP VIEW (looking through)

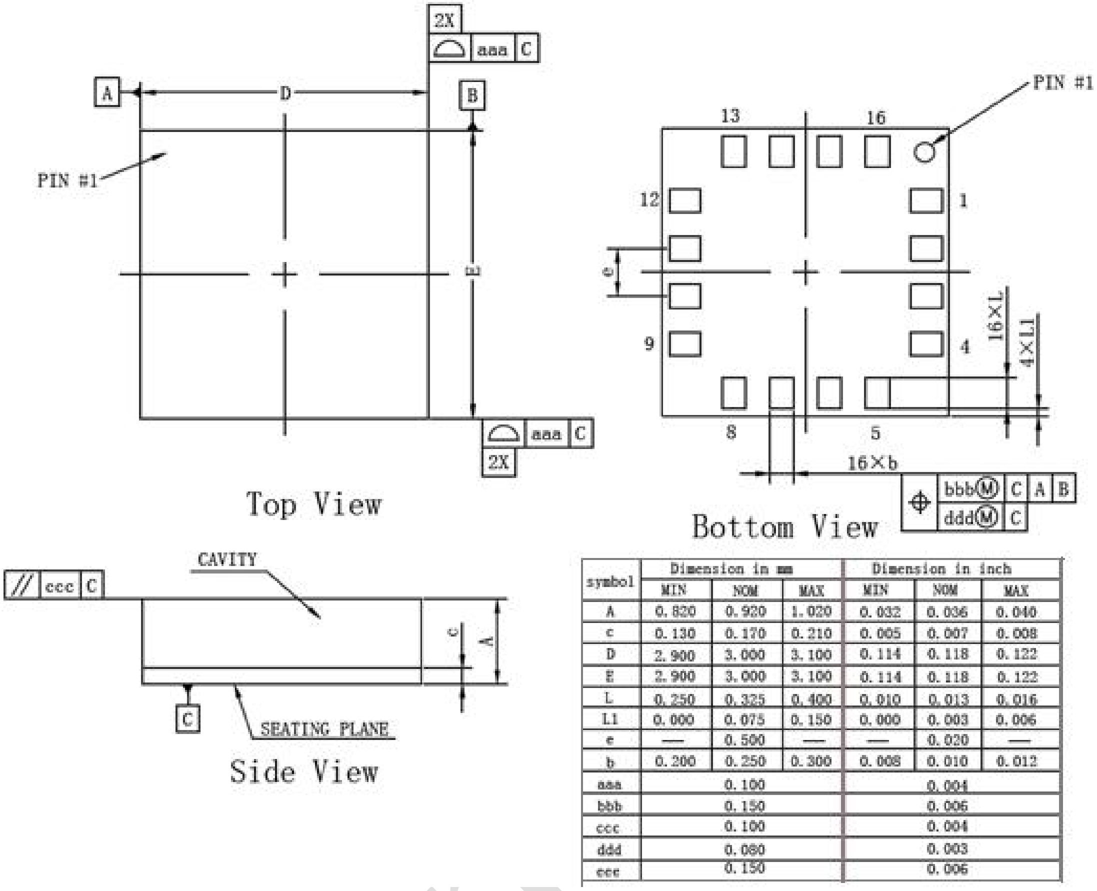
7.2 Package Outlines

7.2.1 Package Type

LGA (Land Grid Array)

7.2.2 Package Size:

3mm (Length)*3mm (Width)*0.9mm (Height)



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.820	0.920	1.020	0.032	0.036	0.040
c	0.130	0.170	0.210	0.005	0.007	0.008
D	2.900	3.000	3.100	0.114	0.118	0.122
E	2.900	3.000	3.100	0.114	0.118	0.122
L	0.250	0.325	0.400	0.010	0.013	0.016
L1	0.000	0.075	0.150	0.000	0.003	0.006
e	—	0.500	—	—	0.020	—
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa		0.100			0.004	
bbb		0.150			0.006	
ccc		0.100			0.004	
ddd		0.080			0.003	
eee		0.150			0.006	

Figure 8. Package Size

7.2.3 Marking:

Tracking code:

Text1: D-Fixed code, C:Version

Text2: VT:Vtran logo

Text3: XXXX:Product Batch Number

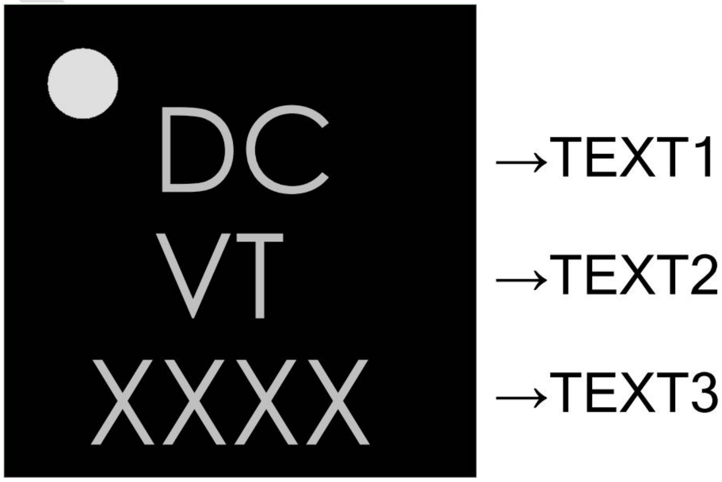


Figure 9. Chip Marking

8 MODES OF OPERATION

8.1 Modes Transition

The device has two different operational modes, controlled by register bit ‘ MODE ‘. The main purpose of the two modes is for power management. The modes can be transited to each other, as shown below, through I^{2}C commands of changing mode bits. The default mode is Standby.

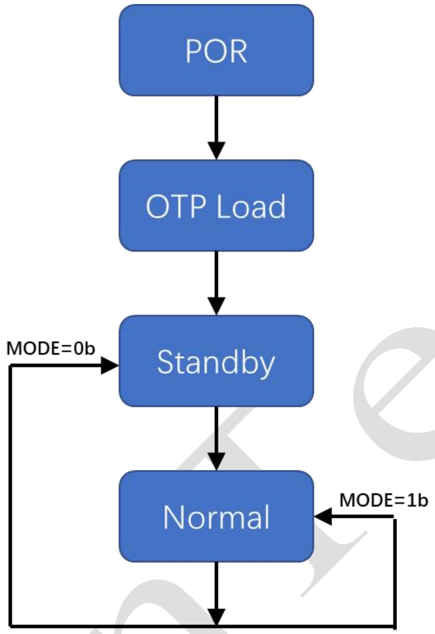


Figure 10. Operation Flow

8.2.1 Read Sequence

Complete magnetometer data read-out can be done as follow steps.

- Data protection, if any of the six data register is accessed, data protection starts. During Data protection period, data register cannot be updated until the last bits 05H have been read.

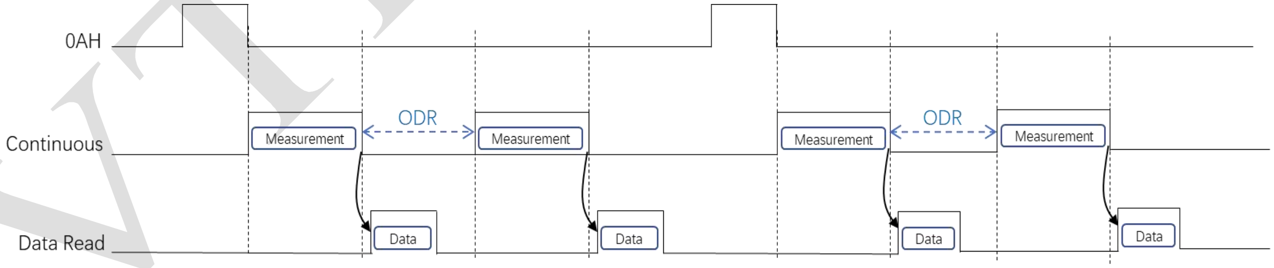


Figure 4. Normal Read Sequence

8.2.2 Standby Mode

Standby mode is the default state of VCM5883L upon Power on、POR and soft reset. In this mode, some block are in normal working state, which make sure the switching mode quickly. In this state, register values are hold on by a low power manager, I^{2}C interface can be woken up by reading or writing any registers. There is no magnetometer measurement in the Standby mode. Internal clocking is also halted.

9 BASIC DEVICE OPERATION

9.1 Anisotropic Magneto-Resistive Sensors

The VCM5883L magneto-resistive sensor circuit consists of tri-axial sensors and application specific support circuits to measure magnetic fields. With a DC power supply is applied to the sensor two terminals, the sensor converts any incident magnetic field in the sensitive axis directions to a differential voltage output. The ASIC then amplifies and processes the signal to have a digital output.

The device has an offset cancellation function to eliminate sensor and ASIC offsets. It also applies a self-aligned magnetic field to restore magnetic state before each measurement to ensure high accuracy. Because of these features, the VCM5883L doesn't need to calibrate every time in most of application situations. It may need to be calibrated once in a new system or a system changes a new battery.

9.2 Power Management

There are two power supply pins to the device. VDD provides power for all the internal analog and digital functional blocks. VDDIO provides power for digital I/O and logic. It is possible to work with VDDIO equal to VDD, the single supply mode, or with VDDIO lower than VDD, the dual supply mode.

The device should turn-on both power pins in order to operate properly. When the device is powered on, all registers are reset by POR, then the device transits to the standby mode and waits for further commands.

Table 5 provides references for four power states. Transitions between power state 2 and power state 3 are prohibited, due to leakage current concerns.

Table 15: Power States

Power State	VDD	VDDIO	Power State description
1	0V	0V	Device Off, No Power Consumption
2	0V	1.65v~3.6v	Device Off, Unpredictable Leakage Current on VDD due to Floating Node.
3	2.16v~3.6v	0	Device Off, Same Current as Standby Mode
4	2.16v~3.6v	1.65v~3.6v	Device On, Normal Operation Mode, Enters Standby Mode after POR

9.3 Power On/Off Time

Table 16. Time Required for Power On/Off

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
POR Completion Time	PORT	Time Period After VDD and VDDIO at Operating Voltage to Ready for I^{2}C Command and Analogy Measurement.			350	μs
Power off Voltage	SDV	Voltage that Device Considers to be Power Down.			0.2	V
Power on Interval	PINT	Time Period Required for Voltage Lower Than SDV to Enable Next POR	100			μs

After the device is powered on, some time periods are required for the device fully functional. The external power supply requires a time period for voltage to ramp up (PSUP), it is typically 50 milli-second. However it isn't controlled by the device. The Power-On-Reset time period (PORT) includes time to reset all the logics, load values in NVM to proper registers, enter the standby mode and get ready for analogy measurements. The power on/off time related to the device is in Table 6.

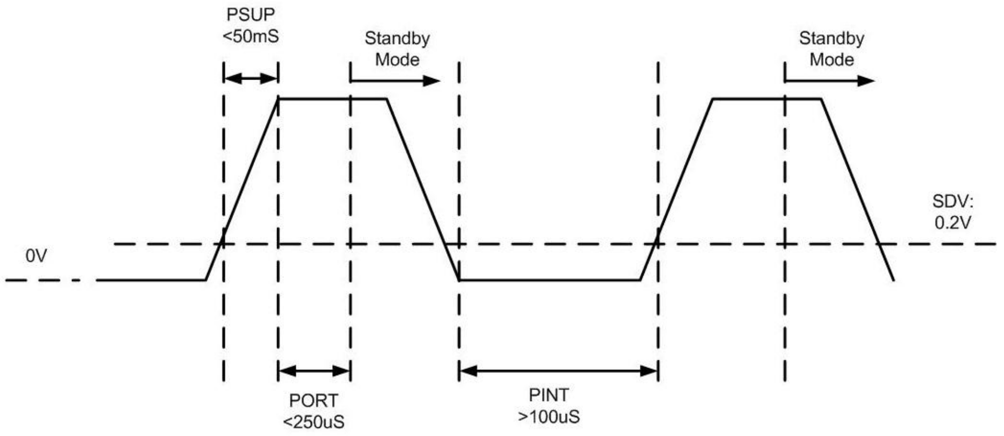


Figure 11. Power On/Off Timing

9.4 Communication Bus Interface I²C

This device will be connected to a serial interface bus as a slave device under the control of a master device, such as the processor. Control of this device is carried out via I²C.

This device is compliant with I²C-Bus Specification, document number: 9398 393 40011. As an I²C compatible device, this device has a 7-bit serial address and supports I²C protocols. This device supports standard and fast speed modes, 100kHz and 400kHz, respectively. External pull-up resistors are required to support all these modes.

9.5 Internal Clock

The device has an internal clock for internal digital logic functions and timing management. This clock is not available to external usage.

ORDERING INFORMATION

Ordering Number	Temperature Range	Package	Packaging
VCM5883L	-40℃~85℃	LGA-16	Tape and Reel: 3k pieces/reel

Caution

This part is sensitive to damage by electrostatic discharge. Use ESD precautionary procedures when touching, removing or inserting.

CAUTION: ESDS CAT. 1B